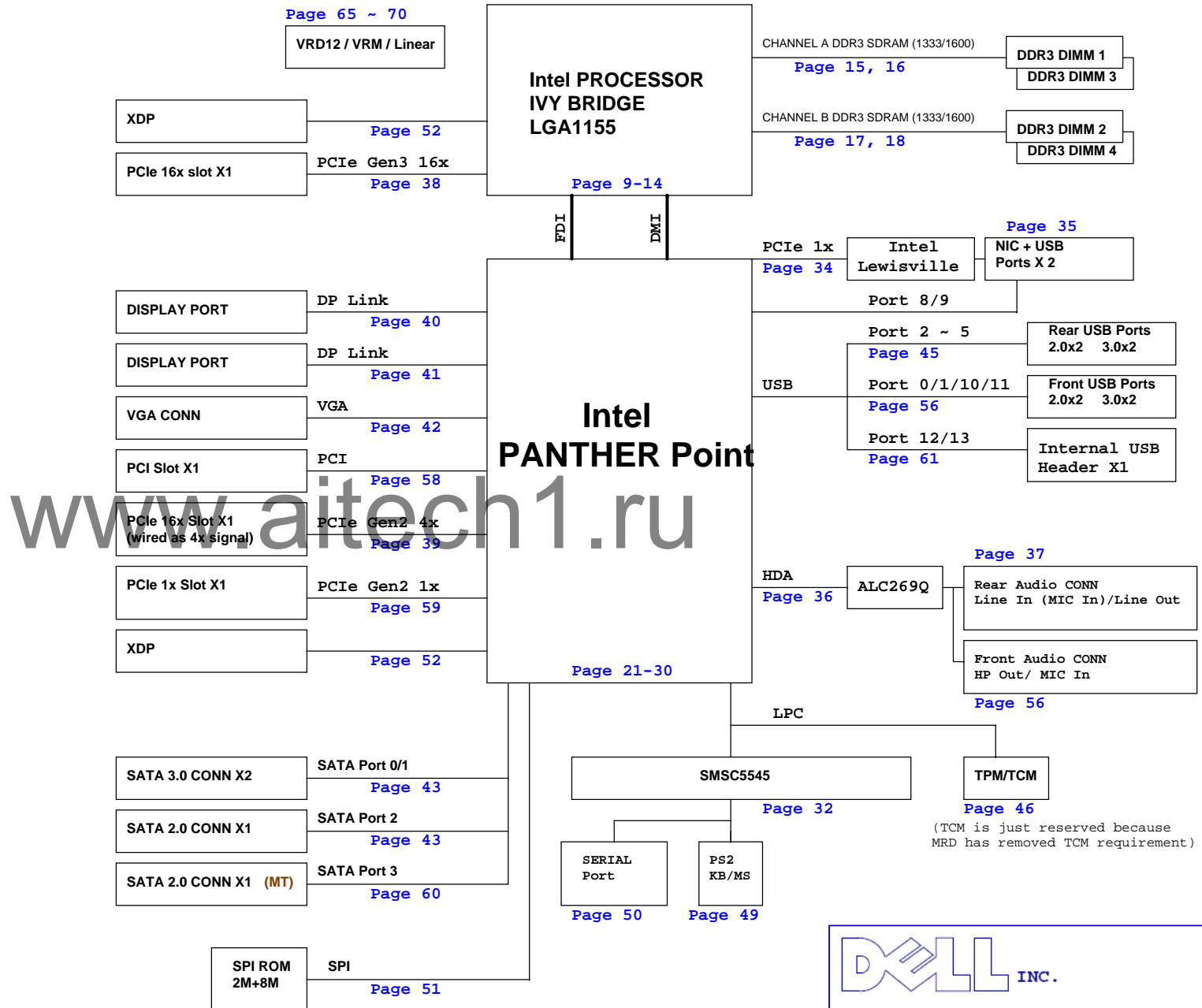


Comoros

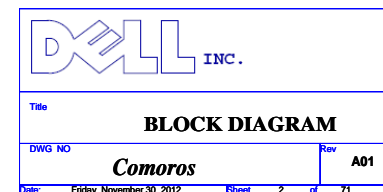
1. Index / Block diagram
2. SMBus MAP
3. Clock Distribution
4. Power Delivery Map
5. Power On Sequence
6. Reset / Power Good Map
7. Strap/IRQ/IDSel Table
8. GPIO Table
- 9-14. CPU
- 15-16. DDR3 Conn: CHA
- 17-18. DDR3 Conn: CHB
19. TBD
20. TBD
- 21-30. PCH
31. PCH MISC Conn/BUZ/ID
- 32-33. SIO:SMSC5544
- 34-35. LAN: INTEL LEWISVILLE
- 36-37 AUDIO:ALC269Q
38. Slot1: PCIe 16x
39. Slot4: PCIe 4x
40. Display Port 1
41. Display Port 2
42. VGA Conn
43. SATA Conn
44. TBD
45. Rear USB
46. TPM & TCM
47. Thermal Sensor Conn
48. FAN
49. PS2 Conn
50. COM1
51. SPI
52. XDP
53. Pilot Run Conn
54. EMI
55. COM2 HDR
56. Front Panel
57. Front USB 3.0
58. Slot3: PCI
59. Slot2: PCIe 1x
60. SATA_MT
61. Flexbay USB
62. TBD
63. Power Conn
64. Power Sequence
- 65-66. Power: Linear Power
- 67-68. Power: Vcore PWM
- 69-70. Power: VCCIO/VCCSA
71. Power: DDR3/5Vdual/5VUSB

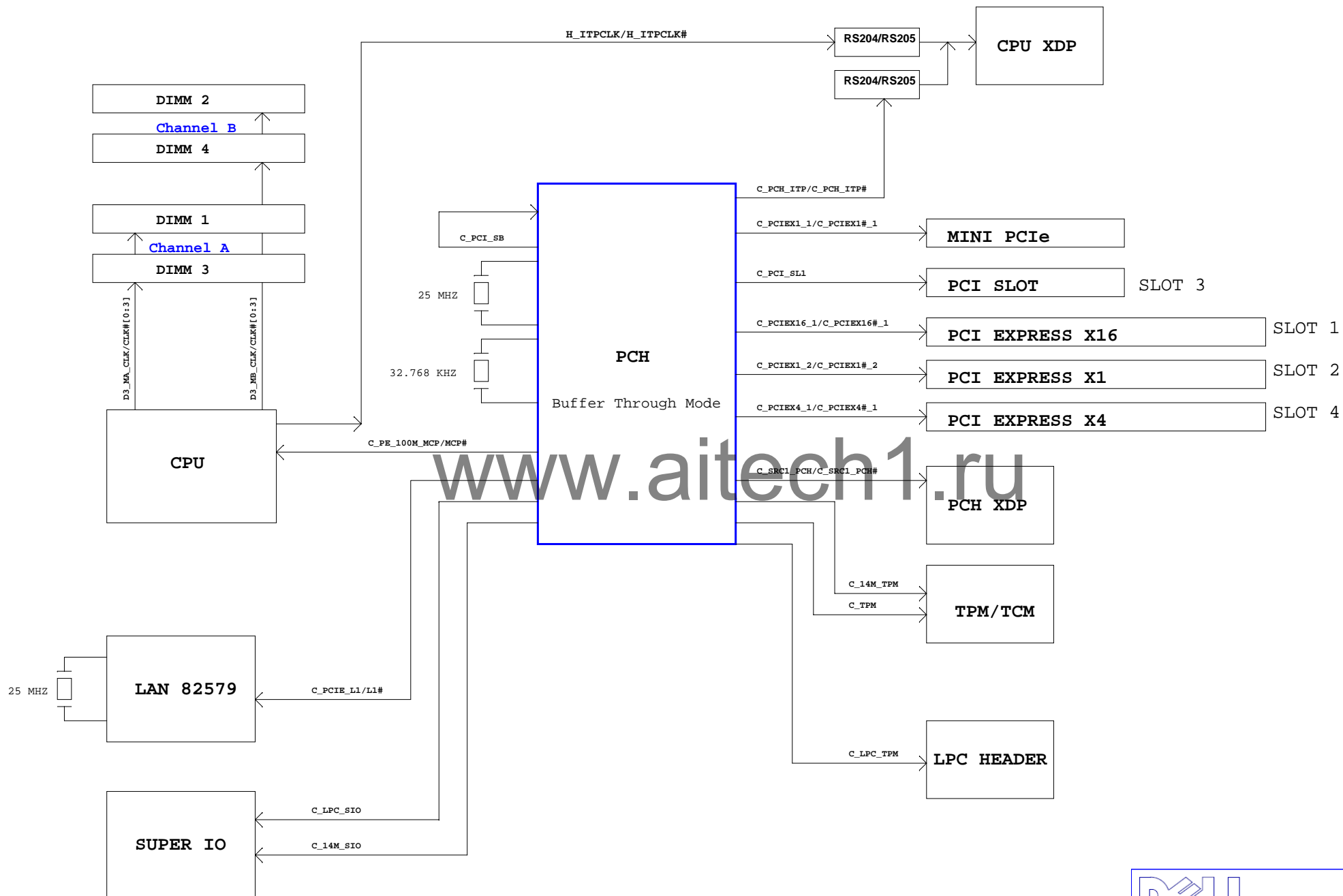


DESIGN	CHECK	APPROVE
Hiko	Hiko	Ivan

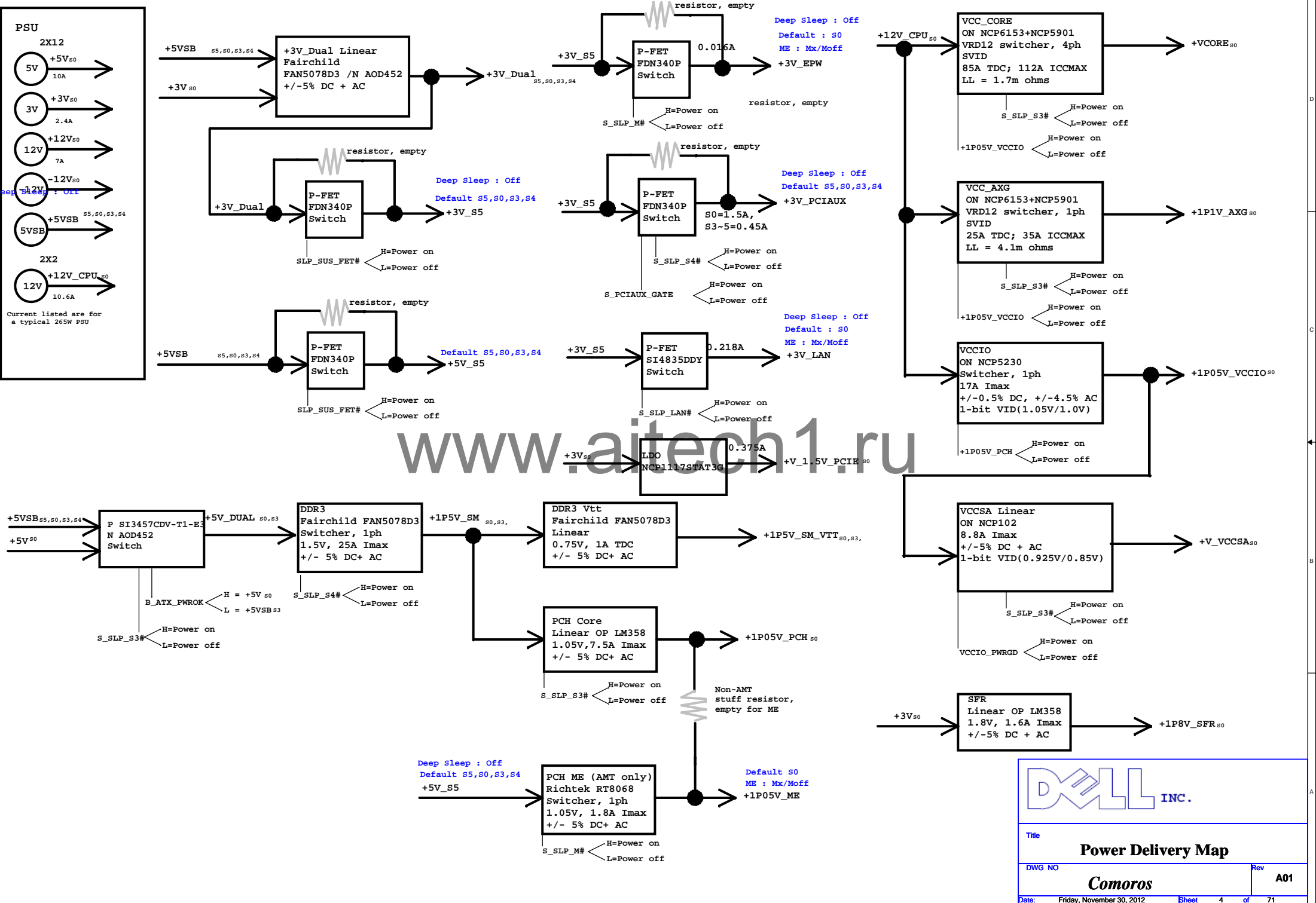
DELL INC.		
Title		
Index / Block diagram		
DWG NO	Rev	A01
Comoros		
Date: Friday, November 30, 2012	Sheet	1 of 71


The diagram shows a large rectangle labeled "PCH" at the bottom. Inside this rectangle is a dashed-line rectangle labeled "SMBus Controller".





POWER DELIVERY MAP

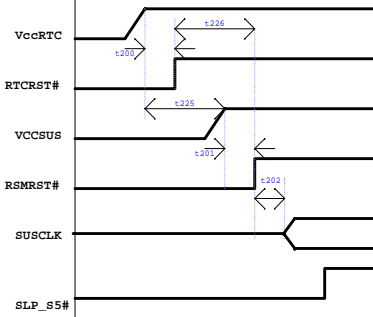


 **INC.**

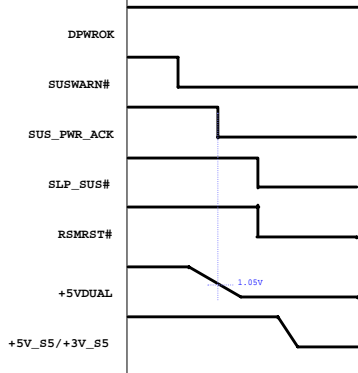
Title		
Power Delivery Map		
DWG NO	Rev	A01
Comoros		
Date: Friday, November 30, 2012	Sheet 4	of 71

POWER ON Timing Diagram

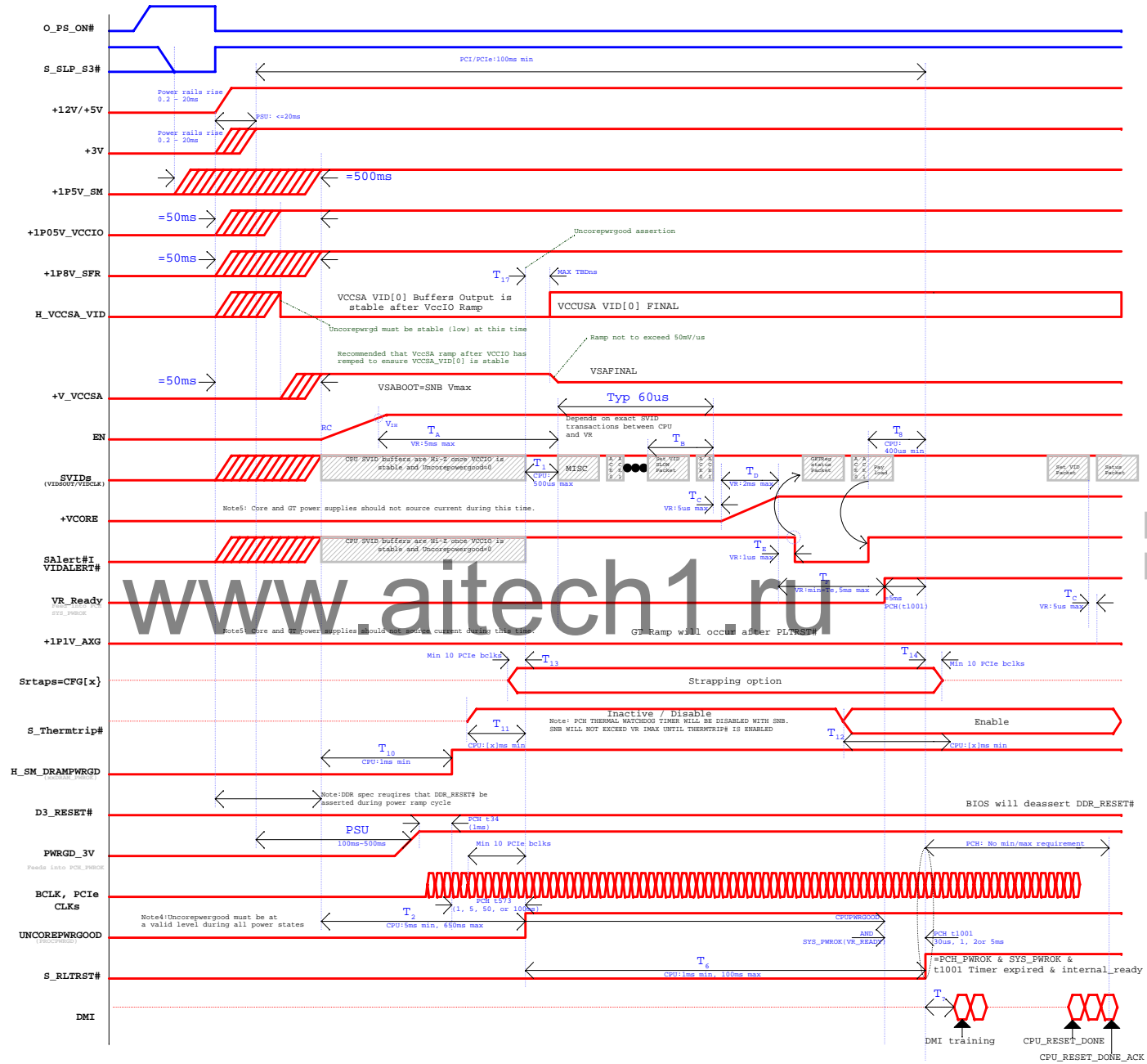
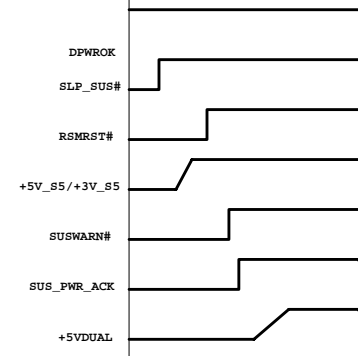
G3 to S4/S5 Timing Diagram



Deep Sleep Entry



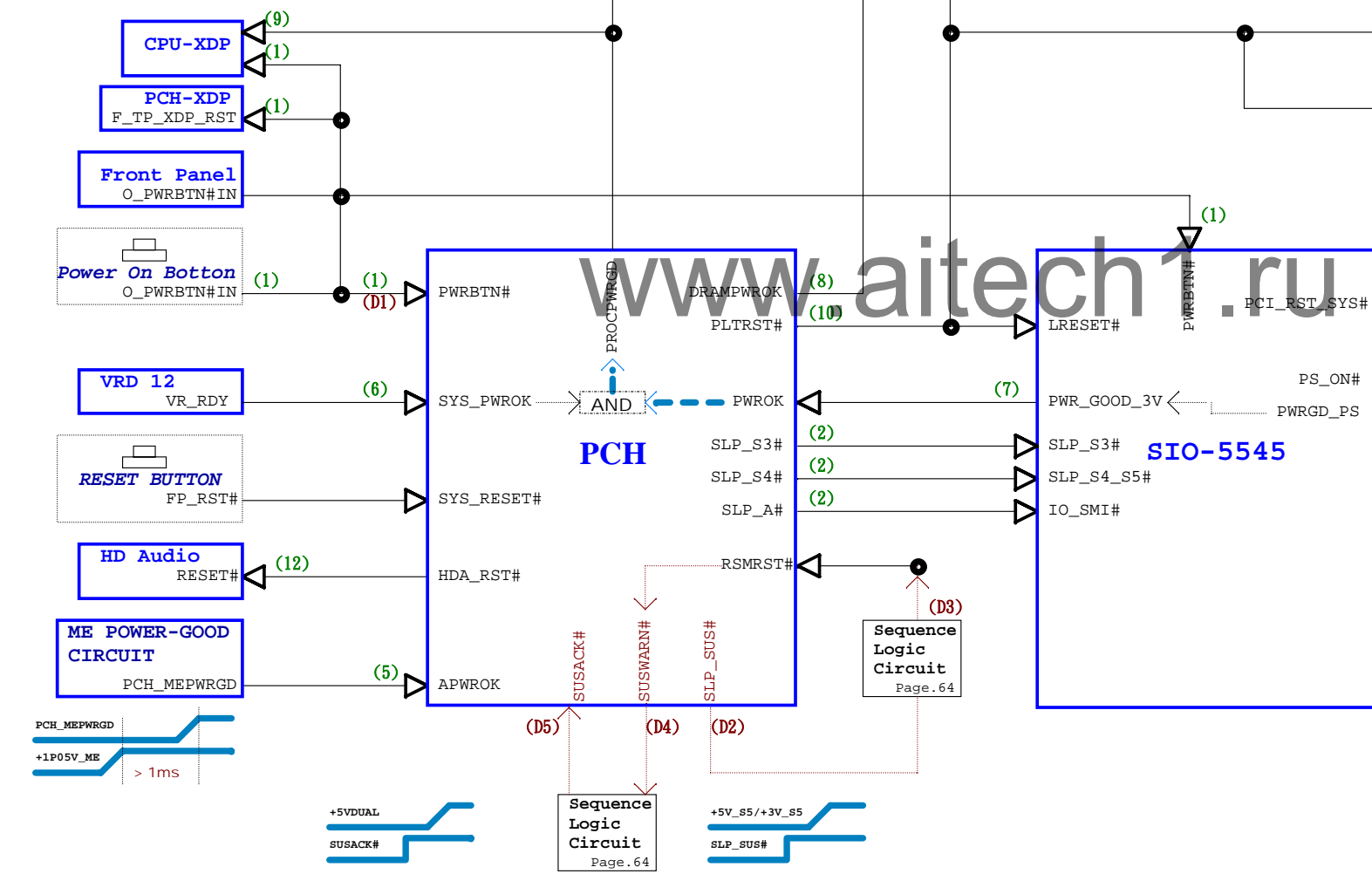
Deep Sleep Exit



RESET / Power Good MAP

Sequence Signal Name:

- (1) O_PWRBTN#IN
- (2) S_SLP_S4# S_SLP_S3# S_SLP_M#
- (3) O_PSON#
- (4) B_ATX_PWROK
- (5) PCH_MEPWRGD
- (6) S_PCH_SYSPWROK P_VR_READY
- (7) PWRGD_3V
- (8) H_DRAMPWROK D3_RESET#
- (9) H_PWRGD
- (10) S_PLTRST# H_RESET#_R S_PLTRST#_R
- (11) X_PLTRST_PCIE_SLOT# K_PCIRST#_SLOT
- (12) A_Z_RST#



Deep Sleep Exit MAP

Sequence Signal Name:

- (D1) O_PWRBTN#IN
- (D2) S_SLP_SUS#
- (D3) S_RSMRST#
- (D4) S_SUSWARN#
- (D5) S_SUS_PWR_ACK#

Title	
Reset / Power Good Map	
DWG NO	Rev
Comoros	A01
Date:	Friday, November 30, 2012
Sheet	6 of 71

IRQ Routing Table

	INTA#	INTB#	INTC#	INTD#	IDSEL	REQn#	GNTn#
Slot3	C	D	A	B	18	0	0

STRAPPING Table

CPU side

CFG[17:0]	Description	
[2]	PCI Express static x16 lane numbering reversal	1: normal Default 0: lane numbers reversed
[6:5]	PCI Express Bifurcation	00: 1x8, 2x4 PCI Express 01: reserved 10: 2x8 PCI Express 11: 1x16 PCI Express Default

PIN NAME	NET		Strapping description
PCI2/TME (PIN4)	C_CK505_33M_PCI2	1	Overclocking DISABLED DEFAULT
		0	Overclocking ENABLED
PCI4/SRC5_EN (PIN6)	C_CK505_33M_PCI4	1	SRC5 DEFAULT
		0	CPU_STOP# and PCI_STOP#
PCIF5/ITP_EN (PIN7)	C_CK505_33M_PCI5	1	CPU_ITP
		0	SRC8 DEFAULT
PCI3/CFGF (PIN5)	C_CK505_33M_PCI3	LOW	See CFG Table DEFAULT (Set SATA and SRC come from PLL4)
		Mid	See CFG Table
		High	See CFG Table

SIO SMSC5545

PIN NAME	NET		Strapping description
GP070 / PWM4 (PIN127)	O_SPEAKER	1	Diag_En Disable
		0	Diag_En Enable DEFAULT
DTR1# [TEST_EN] /GP051 (PIN104)	O_DTR1#_R	1	PE BOOT Loader Strap (DTR1#)= Load from SPI
		0	PE BOOT Loader Strap (DTR1#)= No Load from SPI DEFAULT

PCH

On-Die PLL Voltage Regulator Voltage Select

HDA_SYNC	Description
High	1.5V
Low	1.8V

DEFAULT

On-Die PLL Voltage Regulator

GPIO28 (IN-PU)	Description
High	Regulator is enabled.
Low	Regulator is disabled.

DEFAULT

Topblock Swap Mode

GNT3#/GPIO55 (IN-PU)	Description
High	Topblock swap mode: Disable
Low	Topblock swap mode: Enable

DEFAULT

No Reboot Mode

SPKR (IN-PD)	Description
High	No reboot mode: Enable
Low	No reboot mode: Disable

DEFAULT

Integrated 1.05V VRM

INTVRMEN	Description
High	Integrated 1.05V VRM: Enable
Low	Integrated 1.05V VRM: Disable

DEFAULT

TLS Confidentiality

GPIO15 (IN-PD)	Description
High	ME Crypto TLS cipher suite with confidentiality
Low	ME Crypto TLS cipher suite with no confidentiality

DEFAULT

Flash Descriptor Override Strap

HDA_SDO	Description
High	Flash descriptor security will be override
Low	Disable ME in Manufacturing Mode

DEFAULT

DMI Rx Termination Voltage

SPI_MOSI (IN-PD)	Description
Low	DMI Rx Termination Voltage

DEFAULT

DMI Termination Voltage

NV_CLE (IN-PU)	Description
High	DMI and FDI Tx/Rx Termination Voltage

DEFAULT

Boot BIOS Destination Selection

GNT1# (IN-PU)	SATA1GP/GP19 (IN-PU)	Description
Low	Low	Flash cycle routed to LPC
High	Low	Flash cycle routed to PCI
Low	High	Flash cycle routed to NAND
High	High	Flash cycle routed to SPI

DEFAULT

Deep S4/S5 Well on-die Voltage Regulator Enable

DSWVRMEN	Description
High	Enable
Low	Disable

DEFAULT

Digital Port C Strap

DDPC_CTRLDATA	Description
High	Configure Port C
Low	Disable

DEFAULT



Title
GPIO/IRQ/IDSEL Table

DWG NO
Comoros

Rev
A01

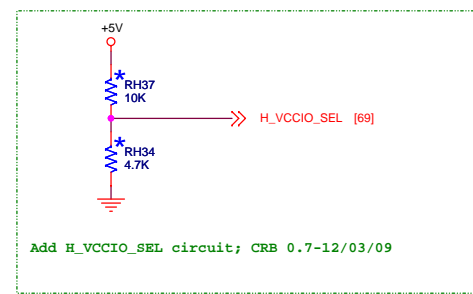
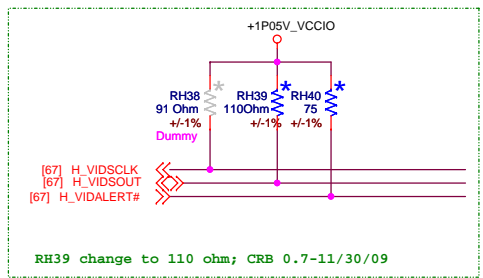
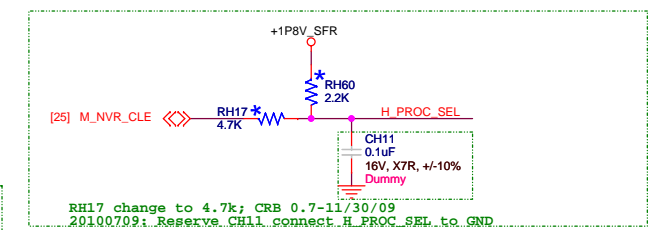
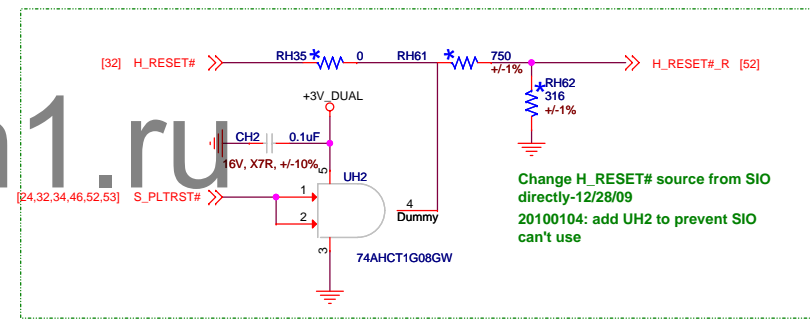
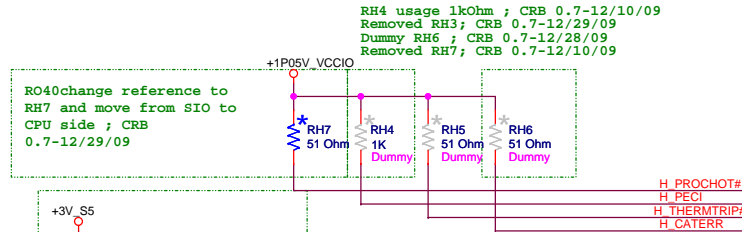
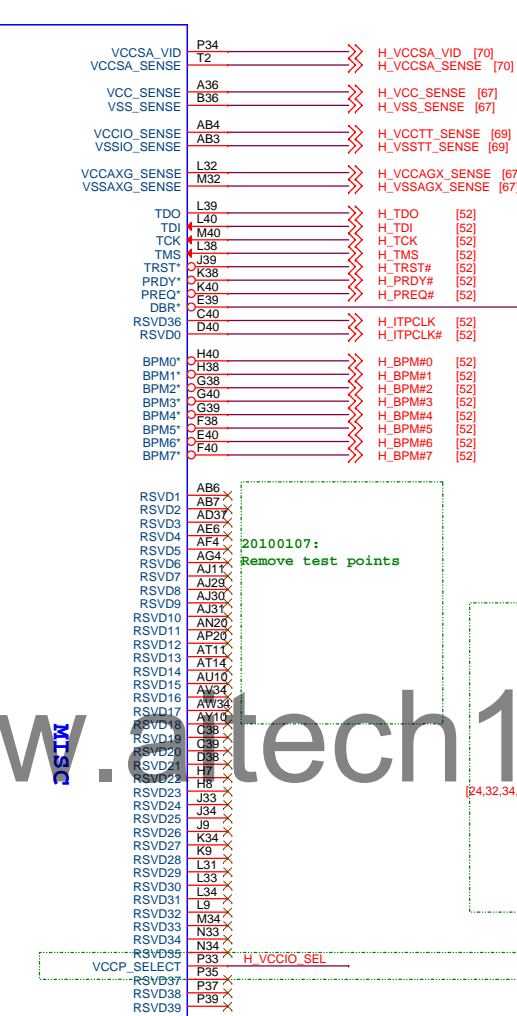
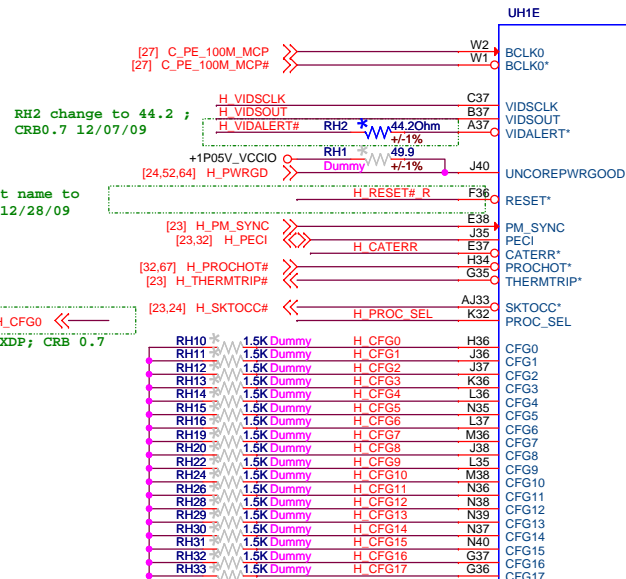
Date: Friday, November 30, 2012 Sheet 7 of 71

PCH GPIO Summary						
GPIO	Type	Power Well	Default	IN-PU/PD	EX-PU/PD	Schematic Usage
GPIO[0]	IO	Core	GPI	--	10k pull-up to +3V	S_PECI_REG#
GPIO[1]	IO	Core	GPI	20K IN-PU (only on TACH1)	10k pull-up to +3V (dummy) 1k pull-down to GND	S_OPL_CHASSIS_ID0
GPIO[2]	IOD	Core	GPI	--	8.2k pull-up to +3V	PCIE_MINI_CPUSS_DETECT#
GPIO[3]	IOD	Core	GPI	--	--	V_DOSP_C_HPD
GPIO[4]	IOD	Core	GPI	--	8.2k pull-up to +3V	V_GPL_VGA_CBL_DET#
GPIO[5]	IOD	Core	GPI	--	8.2k pull-up to +3V	PCIE_MINI_CPPE_DETECT#
GPIO[6]	IO	Core	GPI	20K IN-PU (only on TACH2)	10k pull-up to +3V	S_OPL_PCH_HS_DET#
GPIO[7]	IO	Core	GPI	20K IN-PU (only on TACH3)	10k pull-up to +3V (dummy) 220 pull-down to GND	S_OPL_SKU2
GPIO[8]	IO	Suspend	GPO	20K IN-PU	--	S_TP_0P8
GPIO[9]	IO	Suspend	Native	--	8.2k pull-up to +3V_S5 (dummy)	U_USB_OC_R_#5
GPIO[10]	IO	Suspend	Native	--	10k pull-up to +3V_S5	X_WLAN_WAKE#
GPIO[11]	IO	Suspend	Native	--	10k pull-up to +3V_S5	X4_WAKE#
GPIO[12]	IO	Suspend	Native	--	10k pull-up to +3V_LAN 10k pull-down to GND (dummy)	L_LAN_DISABLE#
GPIO[13]	IO	Suspend	GPI	--	10k pull-up to +3V_S5	X1_WAKE#
GPIO[14]	IO	Suspend	Native	--	8.2k pull-up to +3V_S5	GPO_WLOH
GPIO[15]	IO	Suspend	GPO	20K IN-PD	1k pull-up to +3V_S5 (dummy)	S_PCH_OP15
GPIO[16]	IO	Core	GPI	--	10k pull-up to +3V 10k pull-down to GND (dummy)	H_SKT0CC_R_#
GPIO[17]	IO	Core	GPI	20K IN-PU (only on TACH0)	10k pull-up to +3V (dummy) 1k pull-down to GND	S_OPL_CHASSIS_ID1
GPIO[18]	IO	Core	GPI	20K IN-PU	1k pull-up to +3V (dummy) 1k pull-down to GND (dummy)	S_SATA0P
GPIO[19]	IO	Core	Native	--	10k pull-up to +3V 10k pull-down to GND (dummy)	S_FLEXBAY_HDR_CBL_DET#
GPIO[20]	IO	Core	GPI	--	10k pull-up to +3V (dummy) 10k pull-down to GND	S_OPL_BRD_REV0
GPIO[21]	IO	Core	GPI	--	1k pull-up to +3V 4.7k pull-down to GND (dummy)	S_PCH_CONFIG_JUMPER
GPIO[22]	IO	Core	Native	20K IN-PU	10k pull-up to +3V (dummy)	L_ORG1#
GPIO[24]	IO	Suspend	GPO	--	100k pull-up to +3V_S5	H_SKT0CC#
GPIO[27]	IO	Deep Sleep	GPI	20K IN-PU	10k pull-up to +3V_DUAL 1k pull-down to GND (dummy)	S_OP27_PD
GPIO[28]	IO	Suspend	GPO	20K IN-PU	10k pull-up to +3V_S5 1k pull-down to GND (dummy)	S_PCH_OP28_PU
GPIO[29]	IO	Suspend	Native	--	1k pull-up to +3V_S5 (dummy)	S_SLP_LAN#
GPIO[30]	IO	Deep Sleep	Native	--	10k pull-up to +3V_DUAL (dummy) 1k pull-down to GND (dummy)	S_SUSWARN#
GPIO[31]	IO	Deep Sleep	GPI	TBD IN-PD	8.2k pull-up to +3V_DUAL	S_PSYD_CLR
GPIO[32]	IO	Core	GPO	--	10k pull-up to +3V (dummy) 220 pull-down to GND	S_OPL_SKU0
GPIO[33]	IO	Core	GPO	--	--	--
GPIO[34]	IO	Core	GPI	--	10k pull-up to +3V	PCH_OP1034
GPIO[35]	IO	Core	GPO	--	10k pull-up to +3V (dummy) 220 pull-down to GND	S_OPL_SKU1
GPIO[36]	IO	Core	GPI	20K IN-PD	--	S_PCH_OP36
GPIO[37]	IO	Core	GPI	20K IN-PD	--	S_PCH_OP37
GPIO[38]	IO	Core	GPI	--	10k pull-up to +3V (dummy) 10k pull-down to GND	S_OPL_CHASSIS_ID2
GPIO[39]	IO	Core	GPI	--	10k pull-up to +3V	A_FP_PRES#
GPIO[40]	IO	Suspend	Native	--	--	U_USB_OC_R_#1

GPIO[41]	I/O	Suspend	Native	--	--	U_USB_OC_R_#2
GPIO[42]	I/O	Suspend	Native	--	--	U_USB_OC_R_#3
GPIO[43]	I/O	Suspend	Native	--	8.2k pull-up to +3V_S5 (dummy)	U_USB_OC_R_#4
GPIO[44]	I/O	Suspend	Native	20k IN-PU	10k pull-up to +3V_S5 10k pull-down to GND (dummy)	S_INTRUD_CBL_DET#
GPIO[45]	I/O	Suspend	Native	--	10k pull-up to +3V_S5 10k pull-down to GND (dummy)	O_COM_SER2_DET#
GPIO[46]	I/O	Suspend	Native	20k IN-PU	10k pull-up to +3V_S5 (dummy) 1k pull-down to GND	S_OPL_BRD_REV1
GPIO[48]	I/O	Core	GPI	--	10k pull-up to +3V	S_OPIO48_PU
GPIO[49]	I/O	Core	GPI	--	8.2k pull-up to +3V	TMIN_SHIFT
GPIO[50]	I/O	Core	Native	--	8.2k pull-up to +3V	K_REQ#1
GPIO[51]	I/O	Core	Native	20k IN-PU	1k pull-up to +3V (dummy) 1k pull-down to GND (dummy)	K_ONT#1
GPIO[52]	I/O	Core	Native	--	8.2k pull-up to +3V	K_REQ#2
GPIO[53]	I/O	Core	Native	20k IN-PU	1k pull-down to GND (dummy)	K_ONT#2
GPIO[54]	I/O	Core	Native	--	8.2k pull-up to +3V	K_REQ#3
GPIO[55]	I/O	Core	Native	20k IN-PU	1k pull-down to GND (dummy)	K_ONT#3
GPIO[57]	I/O	Suspend	GPI	--	10k pull-up to +3V_S5 (dummy) 47k pull-down to GND	S_OPIO57_PD
GPIO[58]	I/O	Suspend	Native	--	10k pull-up to +3V_S5	S_SMLINK1_CLK
GPIO[59]	I/O	Suspend	Native	--	--	U_USB_OC_R_#0
GPIO[60]	I/O	Suspend	Native	--	2.2k pull-up to +3V_S5	GPIO_WIRELESS_DISABLE#
GPIO[61]	I/O	Suspend	Native	--	8.2k pull-up to +3V_S5 (dummy)	S_LPCPD#
GPIO[62]	I/O	Suspend	Native	--	--	S_SUSCLK
GPIO[63]	I/O	Suspend	Native	--	10k pull-up to +3V_S5	S_PCIAUX_GATE
GPIO[64]	I/O	Core	Native	20k IN-PD	--	S_TP_CLKOUTFLEX0
GPIO[65]	I/O	Core	Native	20k IN-PD	--	C_14M_SIO_R
GPIO[66]	I/O	Core	Native	20k IN-PD	--	S_TP_CLKOUTFLEX2
GPIO[67]	I/O	Core	Native	20k IN-PD	--	C_14M_TMR_R
GPIO[68]	I/O	Core	GPI	20k IN-PU (only on TACH4)	10k pull-up to +3V (dummy) 220 pull-down to GND	S_OPL_BRD_REV2
GPIO[69]	I/O	Core	GPI	20k IN-PU (only on TACH5)	10k pull-up to +3V	O_PRT_DET#
GPIO[70]	I/O	Core	Native	20k IN-PU (only on TACH6)	8.2k pull-up to +3V	S_FP_CHAS_DET#
GPIO[71]	I/O	Core	Native	20k IN-PU (only on TACH7)	10k pull-up to +3V	--
GPIO[72]	I/O	Suspend	Native (Mobile Only)	20k IN-PU	10k pull-up to +3V_S5	S_PCH_GP72_PU
GPIO[74]	I/O	Suspend	Native	--	10k pull-up to +3V_S5	S_MFG_MODE_OR
GPIO[75]	I/O	Suspend	Native	--	10k pull-up to +3V_S5	S_SMLINK1_DATA

GPIO	PIN NAME	Power well	Buffer Type	EX-PU/PD	Signal Name
OP000	(DIA0_LED0#) OP000	VTR	I/O	NA	O_DIA0_LED0#
OP001	(DIA0_LED1#) OP001	VTR	I/O	NA	O_DIA0_LED1#
OP002	(DIA0_LED2#) OP002	VTR	I/O	NA	O_DIA0_LED2#
OP003	(DIA0_LED4#) OP003	VTR	I/O	NA	O_DIA0_LED4#
OP004	OP004	VTR	I/O	NA	NC
OP005	(H_CUPRST#) OP005 / PECIAL_REQUEST#	VTR	IO/OD	10k pull-up to +3V	O_PECIAL_REQUEST#
OP006	YELLOW# / OP006	VTR	OD/O	NA	O_YELLOW#
OP007	GREEN# / OP007	VTR	OD/O	NA	O_GREEN#
OP010	SMODAT# / OP010	VTR	IODIO	0.2k pull-up to +3V_DUAL (dummy)	S_SMLINK1_DATA_R
OP011	SMBCLK# / OP011	VTR	IODIO	8.2k pull-up to +3V_DUAL (dummy)	S_SMLINK1_CLK_R
OP012	OP012	VTR	I/O	8.2k pull-up to +3V_DUAL	SPL_DI
OP013	OP013	VTR	I/O	NA	NC
OP014	(TMIN_SHIFT) OP014	VTR	I/O	8.2k pull-up to +3V	TMIN_SHIFT
OP015	PWRBTN# / OP015	VTR	I/O	1k pull-up to +3V_DUAL	O_PWRBTN#
OP016	PROCHOT_J# / PROCHOT_OUT# / OP016	VTR	IODIOD	51 ohm pull-up to +1P05V_VCCIO	H_PROCHOT#
OP017	TACH1 / OP017	VTR	I/O	1k pull-up to +3V	O_SEN_CPUFAN
OP020	TACH2 / OP020	VTR	I/O	1k pull-up to +3V	O_SEN_CHAFAN
OP021	TACH3 / OP021	VTR	I/O	NA	NC
OP022	PWM1 / OP022	VTR	OD/O	4.7k pull-up to +3V	O_CPUFAN_PWM
OP023	PWM2 / OP023	VTR	OD/O	4.7k pull-up to +3V	O_CHAFAN_PWM
OP024	PWM3 / OP024	VTR	OD/O	NA	NC
OP025	(FP_CBL_DET#) OP025	VTR	I/O	8.2k pull-up to +3V_S5	O_FP_CBL_DET#
OP026	PCL_RST_S# / OP026	VTR	OD/O	NA	X_PCL_RST_PCL_SL0T#
OP027	PCL_RST_SL0T# / OP027	VTR	OD/O	NA	H_RESET#
OP030	PS_ON# / OP030	VTR	OD/O	4.7k pull-up to +5VSB	O_PSON#
OP031	(PC_SPHR_DET) OP031	VTR	I/O	8.2k pull-up to +3V_DUAL	O_AUD_PCSPHR_DET#
OP032	OP032	VTR	I/O	NA	NC
OP033	PWR_GOOD_3V / OP033	VTR	OD/O	NA	PWRGD_3V
OP034	RSNRST# / OP034	VTR	OD/O	10k pull-down to GND	O_RSNRST#
OP035	OP035	VTR	I/O	8.2k pull-up to +3V_DUAL	O_BC_CLK
OP036	(OP036 / SMB_CLK) OP036	VTR	IO/OD	8.2k pull-up to +3V_DUAL (dummy)	S_SMBCLK_PCL_R
OP040	(OP040 / SMB_DAT1) OP040	VTR	IO/OD	8.2k pull-up to +3V_DUAL (dummy)	S_SMBDATA_PCL_R
OP041	OP041 / IO_FME#	VTR	IO/OD	10k pull-up to +3V_S5	O_IO_FME#
OP042	OP042 / DRV0EN0	VTR	IO/OD	100k pull-up to +3V_DUAL (dummy)	T_ESATA_DET#
OP043	DCD1# / OP043 / MCDAT	VTR	IO/OD	NA	O_DCD1#_R
OP044	DSR1# / OP044 / MCLK	VTR	IO/OD	NA	O_DSR1#_R
OP045	ROD1 / OP045	VTR	I/O	NA	O_ROD1_R
OP046	RTS1# / OP046	VTR	OD/O	NA	O_RTS1#_R
OP047	(SV_PSRNT) OP047 / THD1	VTR	IO/OD	NA	O_THD1_R
OP050	CTS1# / OP050	VTR	I/O	NA	O_CTS1#_R
OP051	DTR1# / TEST_EN# / OP051	VTR	OD/O	8.2k pull-up to +3V_DUAL (dummy) 30k pull-down to GND	O_DTR1#_R
OP052	R11# / OP052	VTR	I/O	NA	O_R11#_R
OP053	OP053 / DCD2#	VTR	IO/OD	2.2k pull-up to +3V	O_DCD2#_R
OP054	OP054 / DSR2#	VTR	IO/OD	2.2k pull-up to +3V	O_DSR2#_R
OP055	OP055 / ROD2	VTR	IO/OD	2.2k pull-up to +3V	O_ROD2_R
OP056	(PWR2_PSRNT) OP056 / RTS2#	VTR	IO/OD	30k pull-up to +3V	O_RTS2#_R
OP057	(MB_RE0_P0) OP057 / TXD2	VTR	IO/OD	30k pull-up to +3V	O_TXD2_R
OP058	OP058 / CTS2#	VTR	IO/OD	2.2k pull-up to +3V	O_CTS2#_R
OP061	(MEM_RE0_P0) OP061 / DTR2#	VTR	IO/OD	30k pull-up to +3V	O_DTR2#_R
OP062	OP062 / R12#	VTR	IO/OD	2.2k pull-up to +3V	O_R12#_R
OP063	OP063 / XBORST#	VTR	IO/OD	10k pull-up to +3V	O_XBORST#
OP064	OP064 / A20M	VTR	IO/OD	10k pull-up to +3V	O_A20M
OP065	SLP_S3# / OP065	VTR	I/O	NA	S_SLP_S3#
OP066	SLP_S4_S5# / OP066	VTR	I/O	NA	S_SLP_S4#
OP067	PWR0D_P0 / OP067	VTR	I/O	1k pull-up to +5V	B_ATT_PWROK
OP070	SPEAKER [DIA0_EN#] / OP070	VTR	OD/O	8.2k pull-up to +3V_DUAL (dummy) 8.2k pull-down to GND	O_SPEAKER
OP071	(SLP_M#) OP071 / IO_SMI#	VTR	IO/OD	NA	S_SLP_M#
OP072	PECL1 / LVSBM_CLK1 / OP072	VTR	PECL/IO/ODIO	1k pull-up to +1P05V_VCCIO (dummy)	H_PEC1_R
OP073	PECL_READY / LVSBM_DAT1 / OP073	VTR	PECL/IO/ODIO	1k pull-up to +1P05V_VCCIO	O_OP73_PU





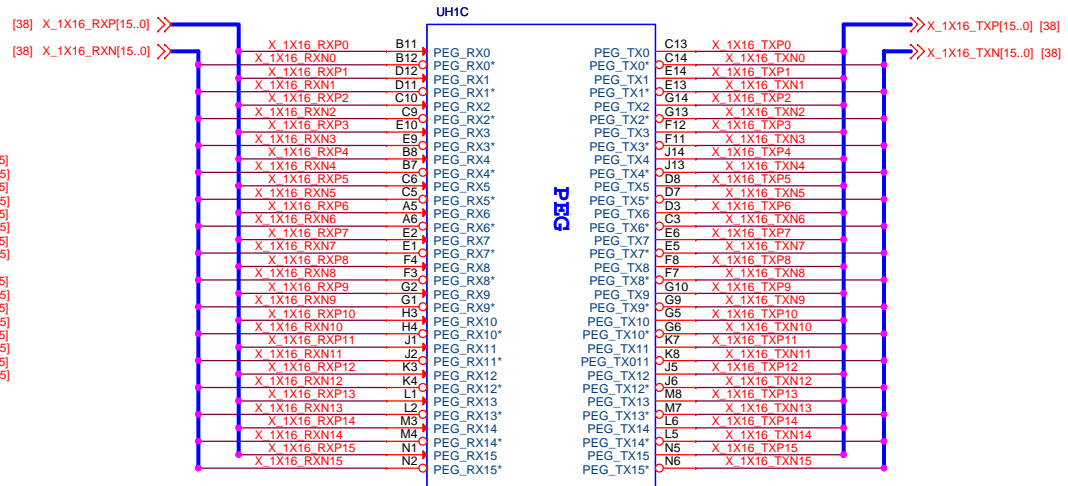
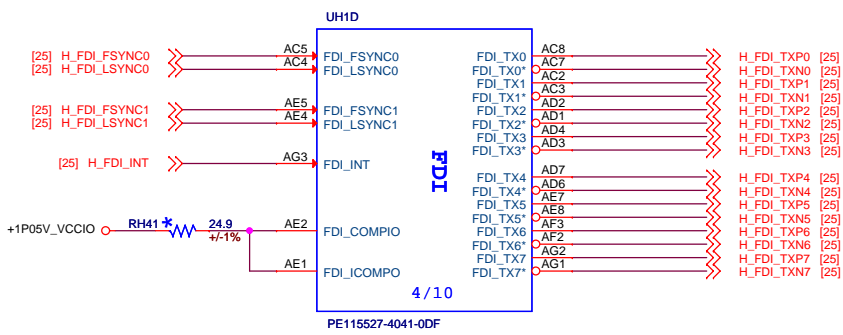
		Title	
		CPU-1: MISC	
DWG NO	Rev	A01	
Date: Friday, November 30, 2012		Sheet	9 of 71

Remove CH1,CH2-12/29/09

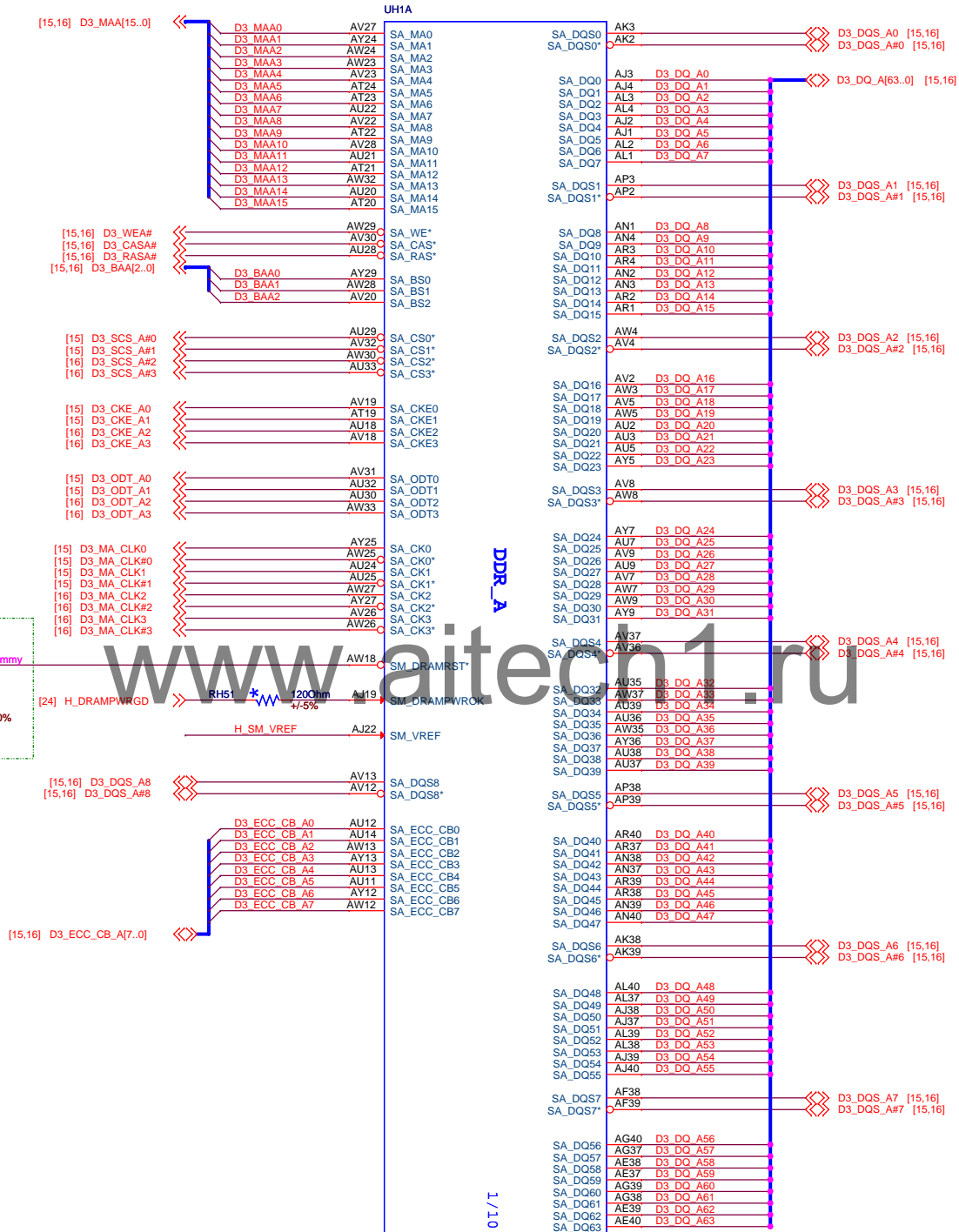
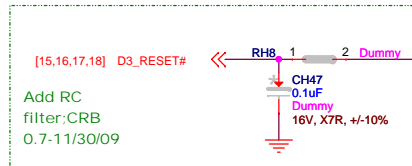
5/10

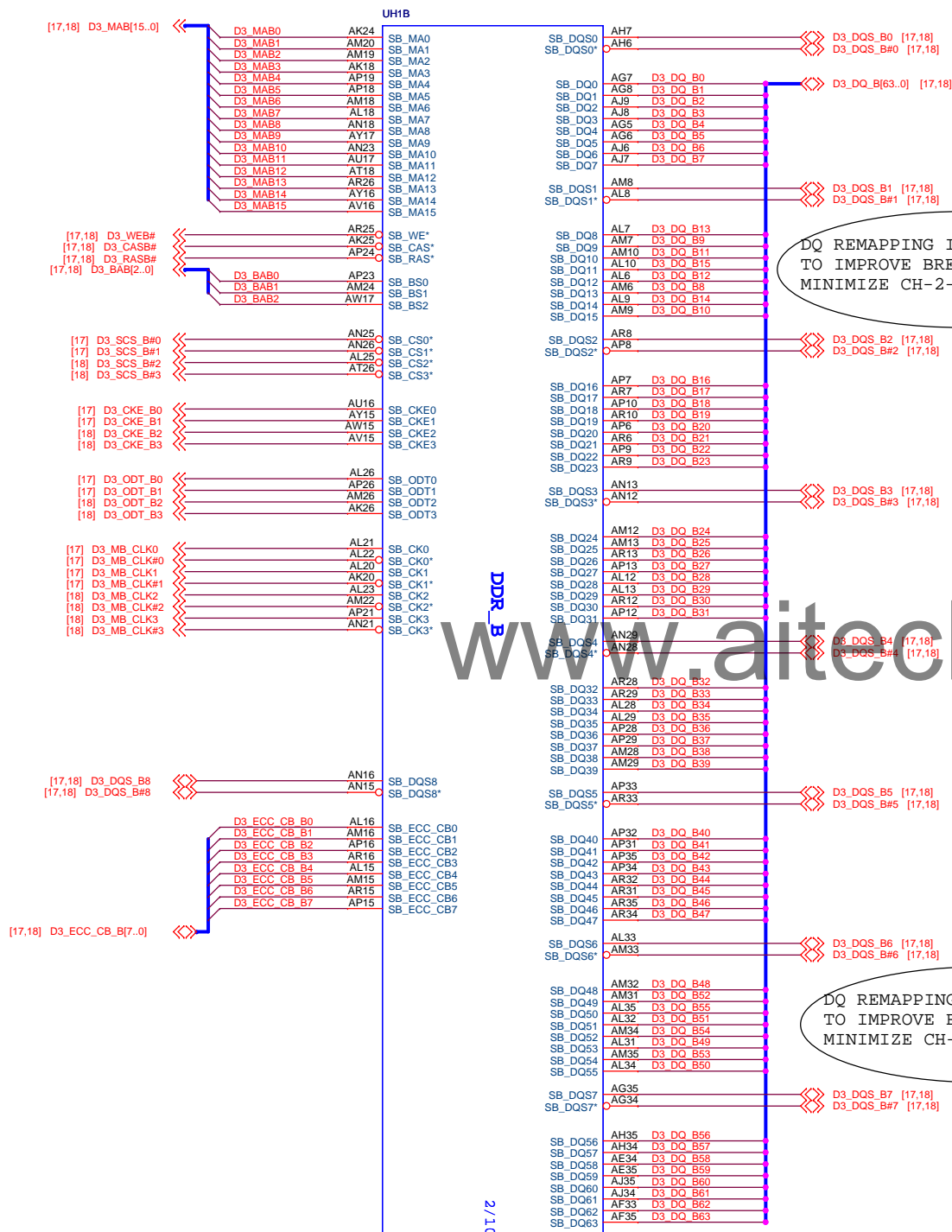
PE115527-4041-ODF

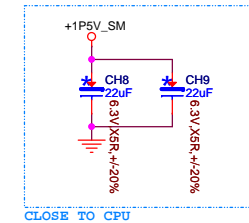
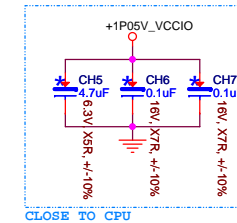
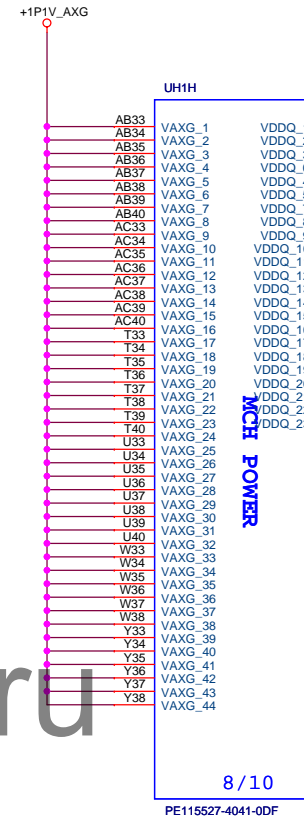
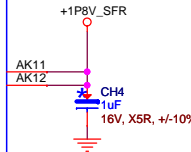
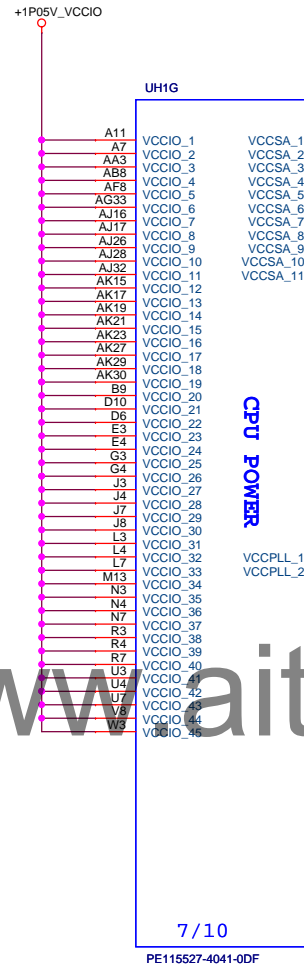
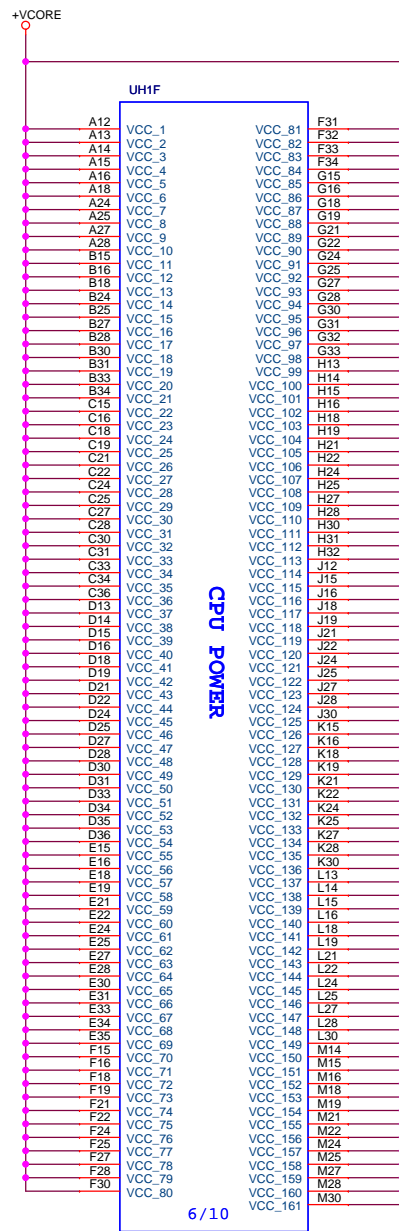
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Title

CPU-5: Power

DWG NO

Comoros

Rev

A01

Date: Friday, November 30, 2012

Sheet 13 of 71

UH11		
A17	VSS_1	VSS_91
A23	VSS_2	VSS_92
A26	VSS_3	VSS_93
A29	VSS_4	VSS_94
A35	VSS_5	VSS_95
AA33	VSS_6	VSS_96
AA34	VSS_7	VSS_97
AA35	VSS_8	VSS_98
AA36	VSS_9	VSS_99
AA37	VSS_10	VSS_100
AA38	VSS_11	VSS_101
AA6	VSS_12	VSS_102
AB5	VSS_13	VSS_103
AC1	VSS_14	VSS_104
AC4	VSS_15	VSS_105
AD33	VSS_16	VSS_106
AD36	VSS_17	VSS_107
AD38	VSS_18	VSS_108
AD39	VSS_19	VSS_109
AD40	VSS_20	VSS_110
AD5	VSS_21	VSS_111
AD6	VSS_22	VSS_112
AE3	VSS_23	VSS_113
AE33	VSS_24	VSS_114
AE36	VSS_25	VSS_115
AF1	VSS_26	VSS_116
AF34	VSS_27	VSS_117
AF36	VSS_28	VSS_118
AF37	VSS_29	VSS_119
AF40	VSS_30	VSS_120
AF5	VSS_31	VSS_121
AF6	VSS_32	VSS_122
AF7	VSS_33	VSS_123
AG36	VSS_34	VSS_124
AH2	VSS_35	VSS_125
AH3	VSS_36	VSS_126
AH33	VSS_37	VSS_127
AH36	VSS_38	VSS_128
AH37	VSS_39	VSS_129
AH38	VSS_40	VSS_130
AH39	VSS_41	VSS_131
AH40	VSS_42	VSS_132
AH5	VSS_43	VSS_133
AH8	VSS_44	VSS_134
AJ12	VSS_45	VSS_135
AJ15	VSS_46	VSS_136
AJ18	VSS_47	VSS_137
AJ21	VSS_48	VSS_138
AJ25	VSS_49	VSS_139
AJ27	VSS_50	VSS_140
AJ36	VSS_51	VSS_141
AJ5	VSS_52	VSS_142
AK1	VSS_53	VSS_143
AK10	VSS_54	VSS_144
AK13	VSS_55	VSS_145
AK14	VSS_56	VSS_146
AK16	VSS_57	VSS_147
AK22	VSS_58	VSS_148
AK28	VSS_59	VSS_149
AK31	VSS_60	VSS_150
AK32	VSS_61	VSS_151
AK33	VSS_62	VSS_152
AK34	VSS_63	VSS_153
AK35	VSS_64	VSS_154
AK36	VSS_65	VSS_155
AK37	VSS_66	VSS_156
AK4	VSS_67	VSS_157
AK40	VSS_68	VSS_158
AK5	VSS_69	VSS_159
AK6	VSS_70	VSS_160
AK7	VSS_71	VSS_161
AK8	VSS_72	VSS_162
AK9	VSS_73	VSS_163
AL11	VSS_74	VSS_164
AL14	VSS_75	VSS_165
AL17	VSS_76	VSS_166
AL19	VSS_77	VSS_167
AL24	VSS_78	VSS_168
AL27	VSS_79	VSS_169
AL30	VSS_80	VSS_170
AL36	VSS_81	
AL5	VSS_82	
AM1	VSS_83	
AM11	VSS_84	
AM14	VSS_85	
AM17	VSS_86	
AM2	VSS_87	
AM21	VSS_88	
AM23	VSS_89	
AM25	VSS_90	

9/10

PE115527-4041-ODF

B39 update to RSVD48;
PDG 0.7-12/07/09

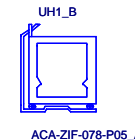
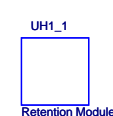
EDS: B39 defined "VSS_NCTF"
CRB: B39 defined "RSVD"

Pin_B39 follow CRB pin define;
CRB 0.7-12/10/09

UH1J		
AT8	VSS_171	VSS_257
AT9	VSS_172	VSS_258
AU1	VSS_173	VSS_259
AU15	VSS_174	VSS_260
AU26	VSS_175	VSS_261
AU34	VSS_176	VSS_262
AU4	VSS_177	VSS_263
AU6	VSS_178	VSS_264
AU40	VSS_179	VSS_265
AV10	VSS_180	VSS_266
AV11	VSS_181	VSS_267
AV14	VSS_182	VSS_268
AV17	VSS_183	VSS_269
AV3	VSS_184	VSS_270
AV35	VSS_185	VSS_271
AV38	VSS_186	VSS_272
AV6	VSS_187	VSS_273
AW10	VSS_188	VSS_274
AW11	VSS_189	VSS_275
AW14	VSS_190	VSS_276
AW16	VSS_191	VSS_277
AW36	VSS_192	VSS_278
AW6	VSS_193	VSS_279
AY11	VSS_194	VSS_280
AY14	VSS_195	VSS_281
AY18	VSS_196	VSS_282
AY35	VSS_197	VSS_283
AY4	VSS_198	VSS_284
AY6	VSS_199	VSS_285
AY8	VSS_200	VSS_286
B10	VSS_201	VSS_287
B13	VSS_202	VSS_288
B14	VSS_203	VSS_289
B17	VSS_204	VSS_290
B23	VSS_205	VSS_291
B26	VSS_206	VSS_292
B29	VSS_207	VSS_293
B32	VSS_208	VSS_294
B35	VSS_209	VSS_295
B38	VSS_210	VSS_296
B6	VSS_211	VSS_297
C11	VSS_212	VSS_298
C12	VSS_213	VSS_299
C17	VSS_214	VSS_300
C20	VSS_215	VSS_301
C23	VSS_216	VSS_302
C26	VSS_217	VSS_303
C29	VSS_218	VSS_304
C32	VSS_219	VSS_305
C35	VSS_220	VSS_306
C7	VSS_221	VSS_307
C8	VSS_222	VSS_308
D17	VSS_223	VSS_309
D2	VSS_224	VSS_310
D20	VSS_225	VSS_311
D23	VSS_226	VSS_312
D26	VSS_227	VSS_313
D29	VSS_228	VSS_314
D32	VSS_229	VSS_315
D37	VSS_230	VSS_316
D39	VSS_231	VSS_317
D4	VSS_232	VSS_318
D5	VSS_233	VSS_319
D9	VSS_234	VSS_320
E11	VSS_235	VSS_321
E12	VSS_236	VSS_322
E17	VSS_237	VSS_323
E20	VSS_238	VSS_324
E23	VSS_239	VSS_325
E26	VSS_240	VSS_326
E29	VSS_241	VSS_327
E32	VSS_242	VSS_328
E36	VSS_243	VSS_329
E7	VSS_244	VSS_330
F1	VSS_245	VSS_331
F10	VSS_246	VSS_332
F13	VSS_247	VSS_333
F14	VSS_248	VSS_334
F17	VSS_249	VSS_335
F2	VSS_250	VSS_336
F20	VSS_251	VSS_337
F23	VSS_252	VSS_338
F26	VSS_253	VSS_339
F29	VSS_254	VSS_340
F35	VSS_255	VSS_341
F35	VSS_256	VSS_342
F35	VSS_257	VSS_343
F35	VSS_258	VSS_344
F35	VSS_259	VSS_345
F35	VSS_260	VSS_346
F35	VSS_261	VSS_347
F35	VSS_262	VSS_348
F35	VSS_263	VSS_349
F35	VSS_264	VSS_350
F35	VSS_265	VSS_351
F35	VSS_266	VSS_352
F35	VSS_267	VSS_353
F35	VSS_268	VSS_354
F35	VSS_269	VSS_355
F35	VSS_270	VSS_356
F35	VSS_271	VSS_357
F35	VSS_272	VSS_358
F35	VSS_273	VSS_359
F35	VSS_274	VSS_360

10/10

PE115527-4041-ODF



<L>BL>



CPU-6: GND	
Title	Rev
DWG NO	A01
Date: Friday, November 30, 2012	
Sheet	14 of 71

SMB ADDRESS:000



SA_BS[0]-->Pin 71 (BA
SA_BS[1]-->Pin 190 (B
SA_BS[2]-->Pin 52 (BA
CRB 0.7-12/10/09

16.17
516.52

3V

CD6
10uF
16V, X5R, +/-10%

CD7
10uF
6.3V, X5R, +/-10%

20100104: Remove CD5 10uF

```

[16,17,18,32,52] S_SMBCLK_MAIN
[16,17,18,32,52] S_SMBDATA_MAIN
-->Pin 71 (BA0) [11,16] D3_BAA[2..0]
-->Pin 190 (BA1)
-->Pin 52 (BA2)
-12/10/09

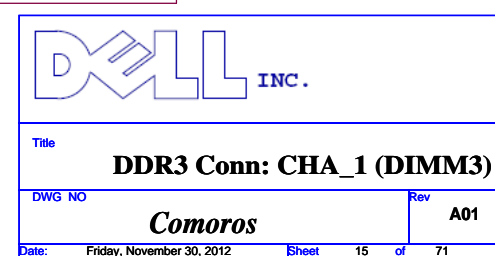
[11] D3_CKE_A#
[11] D3_CKE_A0

[11] D3_SCS_A#
[11] D3_SCS_A#

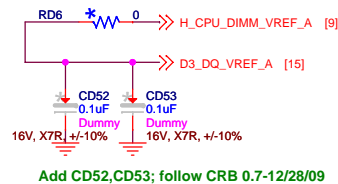
[11] D3_MA_CLK
[11] D3_MA_CLK
[11] D3_MA_CLK
[11] D3_MA_CLK

[11,16] D3_MAA[15..0]

```



SMB ADDRESS:001

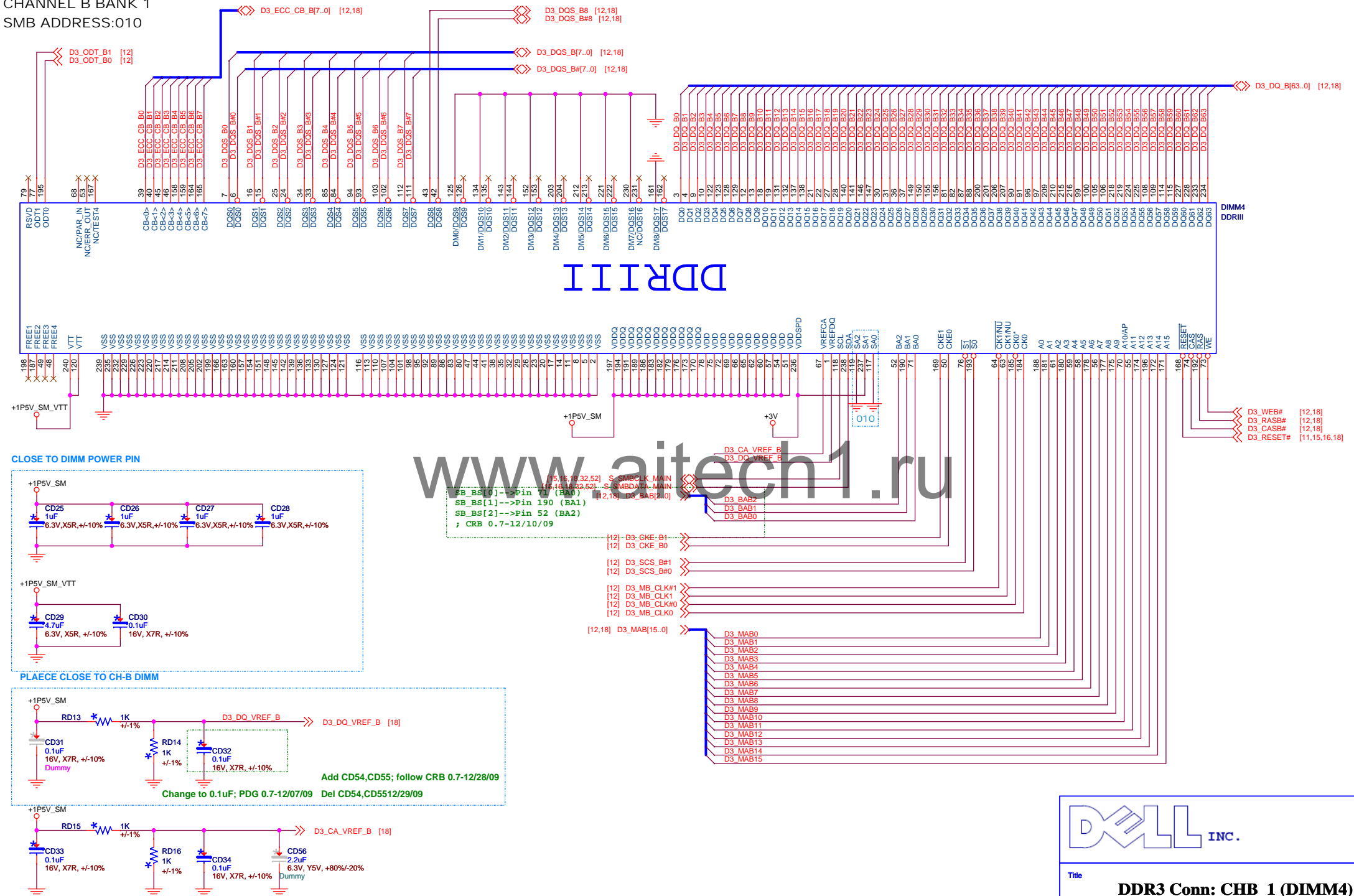
**DDR3 Conn: CHA_2 (DIMM1)**

DWG NO	Rev
	A01

Comoros	A01
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Date: Friday, November 30, 2012 **Sheet** 16 **of** 71

CHANNEL B BANK 1
SMB ADDRESS:010



Title			
DDR3 Conn: CHB_1 (DIMM4)			
DWG NO			Rev
Comoros			A01
Date:	Friday, November 30, 2012	Sheet	17 of 71

SMB ADDRESS:011



20100106: Remove ONFI function since not support

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Title
TBD

DWG NO	Comoros	Rev	A01
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Date:	Friday, November 30, 2012	Sheet	19	of	71
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Title Clock GEN	
DWG NO Comoros	Rev A01
Date: Friday, November 30, 2012 Sheet 20 of 71	

Change AV14 to
K_PCIRST#_SLOT-12/28/09

[58] K_PAR
[58] K_DEVSEL#
[27] C_PCL_S8
[58] K_PCIRST#_SLOT
[58] K_IRDY#
[58] K_PME#
[58] K_SERR#
[58] K_STOP#
[58] K_LOCK#
[58] K_TRDY#
[58] K_PERR#
[58] K_FRAME#

GNT [3:0] have Internal Pull-High to 3.3V

[58] K_GNT#0
[58] K_GNT#1
[58] K_GNT#2
[58] K_GNT#3

[58] K_REQ#0
[58] K_REQ#1
[58] K_REQ#2
[58] K_REQ#3

[58] K_INTA#
[58] K_INTB#
[58] K_INTC#
[58] K_INTD#

[26,41] V_DDSP_C_HPD
[42] V_GPI_VGA_CBL_DET#

PCIE_MINI_CPUSB_DETECT#
PCIE_MINI_CPPE_DETECT#

BH8 PAR
BH9 DEVSEL#
BD15 CLKIN_PCILOOPBACK
AV14 PCIRST#
BF11 IRDY#
BR6 PME#
BC12 SERR#
BA17 STOP#
BC8 PLOCK#
BM3 TRDY#
BC11 PERR#
FRAME#

US1A
BH8 PAR
BH9 DEVSEL#
BD15 CLKIN_PCILOOPBACK
AV14 PCIRST#
BF11 IRDY#
BR6 PME#
BC12 SERR#
BA17 STOP#
BC8 PLOCK#
BM3 TRDY#
BC11 PERR#
FRAME#

GNT0#
GNT1# / GPIO51
GNT2# / GPIO53
GNT3# / GPIO55

REQ0#
REQ1# / GPIO50
REQ2# / GPIO52
REQ3# / GPIO54

PIRQA#
PIRQB#
PIRQC#
PIRQD# / GPIO2
PIRQE# / GPIO3
PIRQF# / GPIO4
PIRQH# / GPIO5

C/BE0#
C/BE1#
C/BE2#
C/BE3#

BN4 K_C/BE#0
BP7 K_C/BE#1
BG2 K_C/BE#2
BP13 K_C/BE#3

AD0 BF15 K_AD0
AD1 BF17 K_AD1
AD2 BT13 K_AD2
AD3 BG12 K_AD3
AD4 BN11 K_AD4
AD5 BJ12 K_AD5
AD6 BU9 K_AD6
AD7 BR12 K_AD7
AD8 BJ3 K_AD8
AD9 BR9 K_AD9
AD10 BJ10 K_AD10
AD11 BM8 K_AD11
AD12 BF3 K_AD12
AD13 BN2 K_AD13
AD14 BE4 K_AD14
AD15 BE6 K_AD15
AD16 BG15 K_AD16
AD17 BC6 K_AD17
AD18 BT11 K_AD18
AD19 BA14 K_AD19
AD20 BL2 K_AD20
AD21 BC4 K_AD21
AD22 BL4 K_AD22
AD23 BC2 K_AD23
AD24 BM13 K_AD24
AD25 BA9 K_AD25
AD26 BF9 K_AD26
AD27 BA8 K_AD27
AD28 BF8 K_AD28
AD29 AV17 K_AD29
AD30 BK12 K_AD30
AD31 K_AD31

AD0 BF15 K_AD0
AD1 BF17 K_AD1
AD2 BT13 K_AD2
AD3 BG12 K_AD3
AD4 BN11 K_AD4
AD5 BJ12 K_AD5
AD6 BU9 K_AD6
AD7 BR12 K_AD7
AD8 BJ3 K_AD8
AD9 BR9 K_AD9
AD10 BJ10 K_AD10
AD11 BM8 K_AD11
AD12 BF3 K_AD12
AD13 BN2 K_AD13
AD14 BE4 K_AD14
AD15 BE6 K_AD15
AD16 BG15 K_AD16
AD17 BC6 K_AD17
AD18 BT11 K_AD18
AD19 BA14 K_AD19
AD20 BL2 K_AD20
AD21 BC4 K_AD21
AD22 BL4 K_AD22
AD23 BC2 K_AD23
AD24 BM13 K_AD24
AD25 BA9 K_AD25
AD26 BF9 K_AD26
AD27 BA8 K_AD27
AD28 BF8 K_AD28
AD29 AV17 K_AD29
AD30 BK12 K_AD30
AD31 K_AD31

AD0 BF15 K_AD0
AD1 BF17 K_AD1
AD2 BT13 K_AD2
AD3 BG12 K_AD3
AD4 BN11 K_AD4
AD5 BJ12 K_AD5
AD6 BU9 K_AD6
AD7 BR12 K_AD7
AD8 BJ3 K_AD8
AD9 BR9 K_AD9
AD10 BJ10 K_AD10
AD11 BM8 K_AD11
AD12 BF3 K_AD12
AD13 BN2 K_AD13
AD14 BE4 K_AD14
AD15 BE6 K_AD15
AD16 BG15 K_AD16
AD17 BC6 K_AD17
AD18 BT11 K_AD18
AD19 BA14 K_AD19
AD20 BL2 K_AD20
AD21 BC4 K_AD21
AD22 BL4 K_AD22
AD23 BC2 K_AD23
AD24 BM13 K_AD24
AD25 BA9 K_AD25
AD26 BF9 K_AD26
AD27 BA8 K_AD27
AD28 BF8 K_AD28
AD29 AV17 K_AD29
AD30 BK12 K_AD30
AD31 K_AD31

AD0 BF15 K_AD0
AD1 BF17 K_AD1
AD2 BT13 K_AD2
AD3 BG12 K_AD3
AD4 BN11 K_AD4
AD5 BJ12 K_AD5
AD6 BU9 K_AD6
AD7 BR12 K_AD7
AD8 BJ3 K_AD8
AD9 BR9 K_AD9
AD10 BJ10 K_AD10
AD11 BM8 K_AD11
AD12 BF3 K_AD12
AD13 BN2 K_AD13
AD14 BE4 K_AD14
AD15 BE6 K_AD15
AD16 BG15 K_AD16
AD17 BC6 K_AD17
AD18 BT11 K_AD18
AD19 BA14 K_AD19
AD20 BL2 K_AD20
AD21 BC4 K_AD21
AD22 BL4 K_AD22
AD23 BC2 K_AD23
AD24 BM13 K_AD24
AD25 BA9 K_AD25
AD26 BF9 K_AD26
AD27 BA8 K_AD27
AD28 BF8 K_AD28
AD29 AV17 K_AD29
AD30 BK12 K_AD30
AD31 K_AD31

AD0 BF15 K_AD0
AD1 BF17 K_AD1
AD2 BT13 K_AD2
AD3 BG12 K_AD3
AD4 BN11 K_AD4
AD5 BJ12 K_AD5
AD6 BU9 K_AD6
AD7 BR12 K_AD7
AD8 BJ3 K_AD8
AD9 BR9 K_AD9
AD10 BJ10 K_AD10
AD11 BM8 K_AD11
AD12 BF3 K_AD12
AD13 BN2 K_AD13
AD14 BE4 K_AD14
AD15 BE6 K_AD15
AD16 BG15 K_AD16
AD17 BC6 K_AD17
AD18 BT11 K_AD18
AD19 BA14 K_AD19
AD20 BL2 K_AD20
AD21 BC4 K_AD21
AD22 BL4 K_AD22
AD23 BC2 K_AD23
AD24 BM13 K_AD24
AD25 BA9 K_AD25
AD26 BF9 K_AD26
AD27 BA8 K_AD27
AD28 BF8 K_AD28
AD29 AV17 K_AD29
AD30 BK12 K_AD30
AD31 K_AD31

AD0 BF15 K_AD0
AD1 BF17 K_AD1
AD2 BT13 K_AD2
AD3 BG12 K_AD3
AD4 BN11 K_AD4
AD5 BJ12 K_AD5
AD6 BU9 K_AD6
AD7 BR12 K_AD7
AD8 BJ3 K_AD8
AD9 BR9 K_AD9
AD10 BJ10 K_AD10
AD11 BM8 K_AD11
AD12 BF3 K_AD12
AD13 BN2 K_AD13
AD14 BE4 K_AD14
AD15 BE6 K_AD15
AD16 BG15 K_AD16
AD17 BC6 K_AD17
AD18 BT11 K_AD18
AD19 BA14 K_AD19
AD20 BL2 K_AD20
AD21 BC4 K_AD21
AD22 BL4 K_AD22
AD23 BC2 K_AD23
AD24 BM13 K_AD24
AD25 BA9 K_AD25
AD26 BF9 K_AD26
AD27 BA8 K_AD27
AD28 BF8 K_AD28
AD29 AV17 K_AD29
AD30 BK12 K_AD30
AD31 K_AD31

K_AD[31..0] [58]

K_C/BE[3..0] [58]

K_C/BE[3..0] [58]

K_C/BE[3..0] [58]

K_C/BE[3..0] [58]

K_C/BE[3..0] [58]

K_C/BE[3..0] [58]

K_C/BE[3..0] [58]

K_C/BE[3..0] [58]

K_C/BE[3..0] [58]

K_C/BE[3..0] [58]

K_C/BE[3..0] [58]

K_C/BE[3..0] [58]

K_C/BE[3..0] [58]

K_C/BE[3..0] [58]

K_C/BE[3..0] [58]

K_C/BE[3..0] [58]

K_C/BE[3..0] [58]

K_C/BE[3..0] [58]

K_C/BE[3..0] [58]

K_C/BE[3..0] [58]

K_C/BE[3..0] [58]

K_C/BE[3..0] [58]

K_INTA#
K_INTB#
K_INTC#
K_INTD#

PCIE_MINI_CPUSB_DETECT#
V_GPI_VGA_CBL_DET#
PCIE_MINI_CPPE_DETECT#

K_REQ#0
K_REQ#1
K_REQ#2
K_REQ#3

K_FRAME#
K_IRDY#
K_TRDY#
K_DEVSEL#

K_STOP#
K_LOCK#
K_PERR#
K_SERR#

K_STOP#
K_LOCK#
K_PERR#
K_SERR#

K_STOP#
K_LOCK#
K_PERR#
K_SERR#

K_STOP#
K_LOCK#
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K_SERR#

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K_PERR#
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K_STOP#
K_LOCK#
K_PERR#
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K_STOP#
K_LOCK#
K_PERR#
K_SERR#

K_STOP#
K_LOCK#
K_PERR#
K_SERR#

K_INTA#
K_INTB#
K_INTC#
K_INTD#

PCIE_MINI_CPUSB_DETECT#
V_GPI_VGA_CBL_DET#
PCIE_MINI_CPPE_DETECT#

K_REQ#0
K_REQ#1
K_REQ#2
K_REQ#3

K_FRAME#
K_IRDY#
K_TRDY#
K_DEVSEL#

K_STOP#
K_LOCK#
K_PERR#
K_SERR#

K_STOP#
K_LOCK#
K_PERR#
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K_STOP#
K_LOCK#
K_PERR#
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K_PERR#
K_SERR#

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K_PERR#
K_SERR#

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K_SERR#

K_STOP#
K_LOCK#
K_PERR#
K_SERR#

K_STOP#
K_LOCK#
K_PERR#
K_SERR#

K_STOP#
K_LOCK#
K_PERR#
K_SERR#

K_STOP#
K_LOCK#
K_PERR#
K_SERR#

K_STOP#
K_LOCK#
K_PERR#
K_SERR#

K_STOP#
K_LOCK#
K_PERR#
K_SERR#

K_STOP#
K_LOCK#
K_PERR#
K_SERR#

K_STOP#
K_LOCK#
K_PERR#
K_SERR#

K_INTA#
K_INTB#
K_INTC#
K_INTD#

PCIE_MINI_CPUSB_DETECT#
V_GPI_VGA_CBL_DET#
PCIE_MINI_CPPE_DETECT#

K_REQ#0
K_REQ#1
K_REQ#2
K_REQ#3

K_FRAME#
K_IRDY#
K_TRDY#
K_DEVSEL#

K_STOP#
K_LOCK#
K_PERR#
K_SERR#

K_STOP#
K_LOCK#
K_PERR#
K_SERR#

K_STOP#
K_LOCK#
K_PERR#
K_SERR#

K_STOP#
K_LOCK#
K_PERR#
K_SERR#

K_STOP#
K_LOCK#
K_PERR#
K_SERR#

K_STOP#
K_LOCK#
K_PERR#
K_SERR#

K_STOP#
K_LOCK#
K_PERR#
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K_PERR#
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K_SERR#

K_STOP#
K_LOCK#
K_PERR#
K_SERR#

K_STOP#
K_LOCK#
K_PERR#
K_SERR#

K_STOP#
K_LOCK#
K_PERR#
K_SERR#

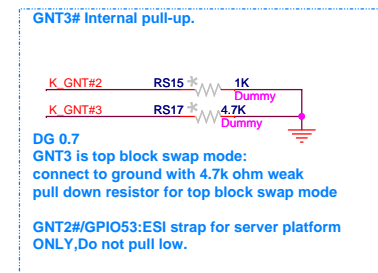
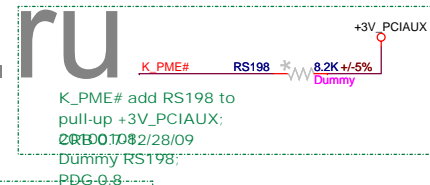
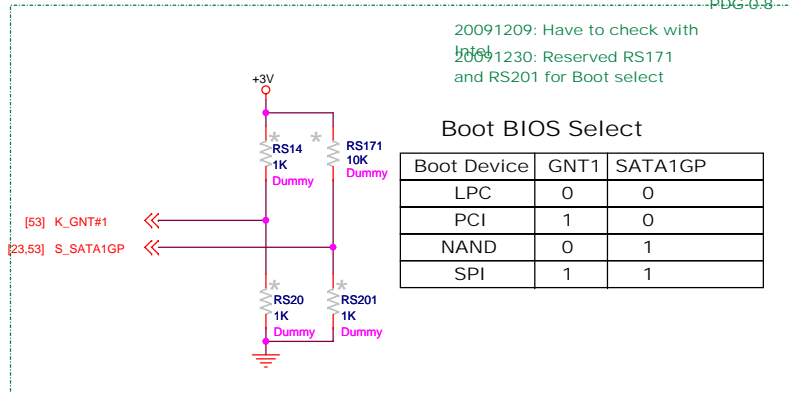
K_STOP#
K_LOCK#
K_PERR#
K_SERR#

K_STOP#
K_LOCK#
K_PERR#
K_SERR#

K_STOP#
K_LOCK#
K_PERR#
K_SERR#

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Left biotth SATA/GPIO19 and GNT1# floating.
No pull up required for Default(SPI)



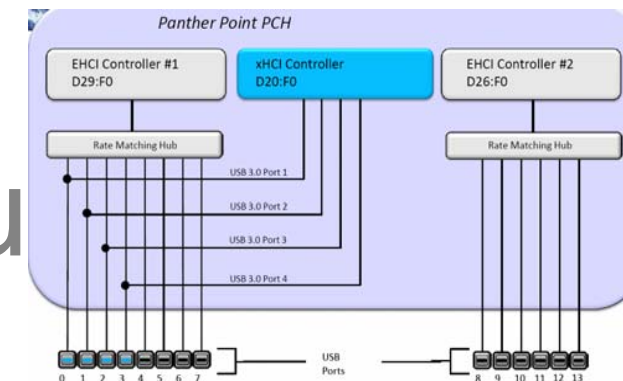
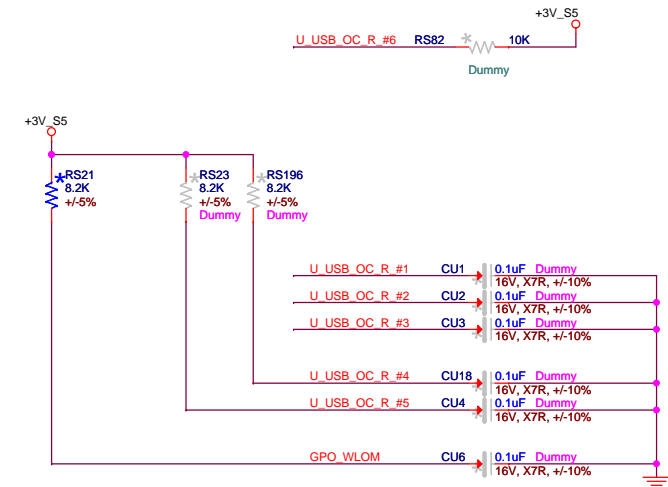
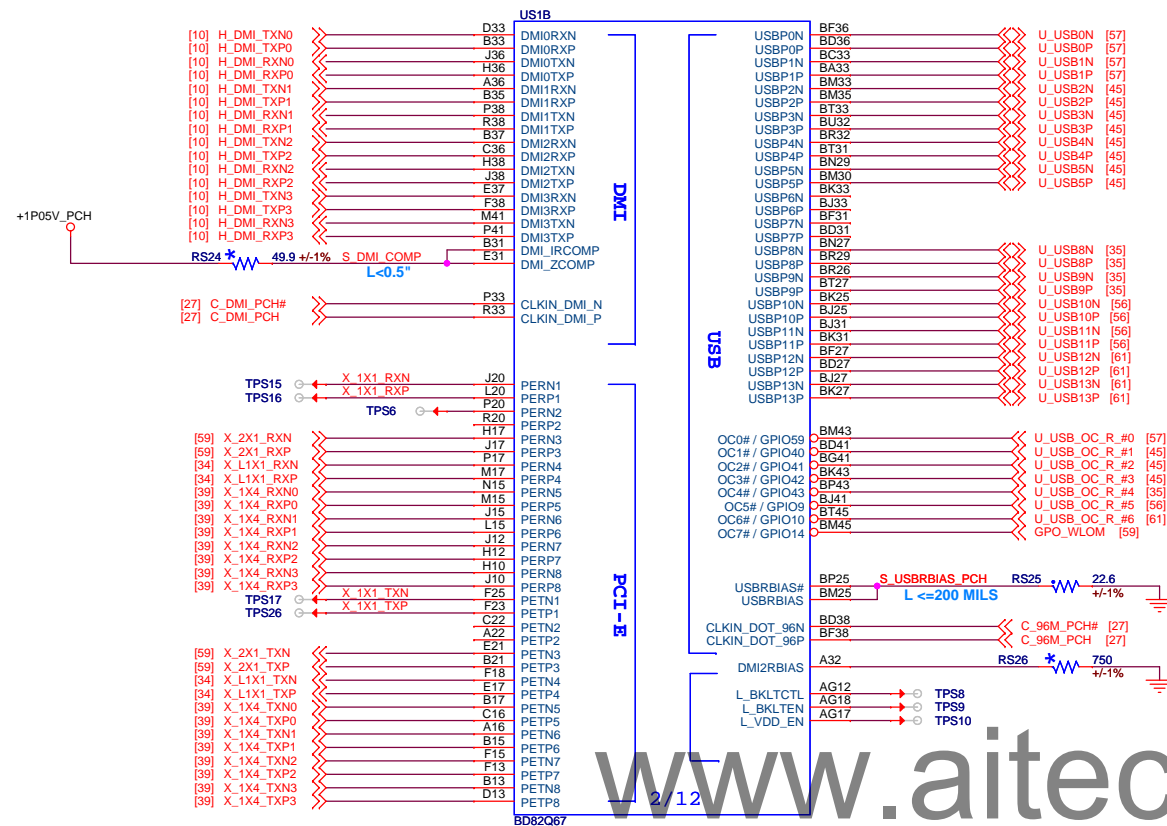
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Title
PCH-1: PCI

DWG NO
Comoros

Rev
A01

Date: Friday, November 30, 2012 Sheet 21 of 71



USB2.0	USB3.0	Lainikai OC Pin	Power	Function	Standard OC pin configuration
Port 0	U_USB0N U_USB0P	Port 1	USBPWR1_F_50	Front USB3.0	OC0#
Port 1	U_USB1N U_USB1P	Port 2	USBPWR2_F_50	Front USB3.0	OC0#
Port 2	U_USB2N U_USB2P	Port 3	U_USB_OC_R_#1	Rear USB3.0	OC1#
Port 3	U_USB3N U_USB3P	Port 4	U_USB_OC_R_#2	Rear USB3.0	OC1#
Port 4	U_USB4N U_USB4P		U_USB_OC_R_#3	Rear USB2.0	OC2#
Port 5	U_USB5N U_USB5P		U_USB_OC_R_#3	Rear USB2.0	OC2#
Port 6	U_USB6N U_USB6P		U_USB_OC_R_#3	Rear USB2.0	OC2#
Port 7	U_USB7N U_USB7P		U_USB_OC_R_#3	Rear USB2.0	OC2#
Port 8	U_USB8N U_USB8P		U_USB_OC_R_#3	Rear USB2.0	OC2#
Port 9	U_USB9N U_USB9P		U_USB_OC_R_#3	Rear USB2.0	OC2#
Port 10	U_USB10N U_USB10P		U_USB_OC_R_#3	Rear USB2.0	OC2#
Port 11	U_USB11N U_USB11P		U_USB_OC_R_#3	Rear USB2.0	OC2#
Port 12	U_USB12N U_USB12P		U_USB_OC_R_#3	Rear USB2.0	OC2#
Port 13	U_USB13N U_USB13P		U_USB_OC_R_#3	Rear USB2.0	OC2#

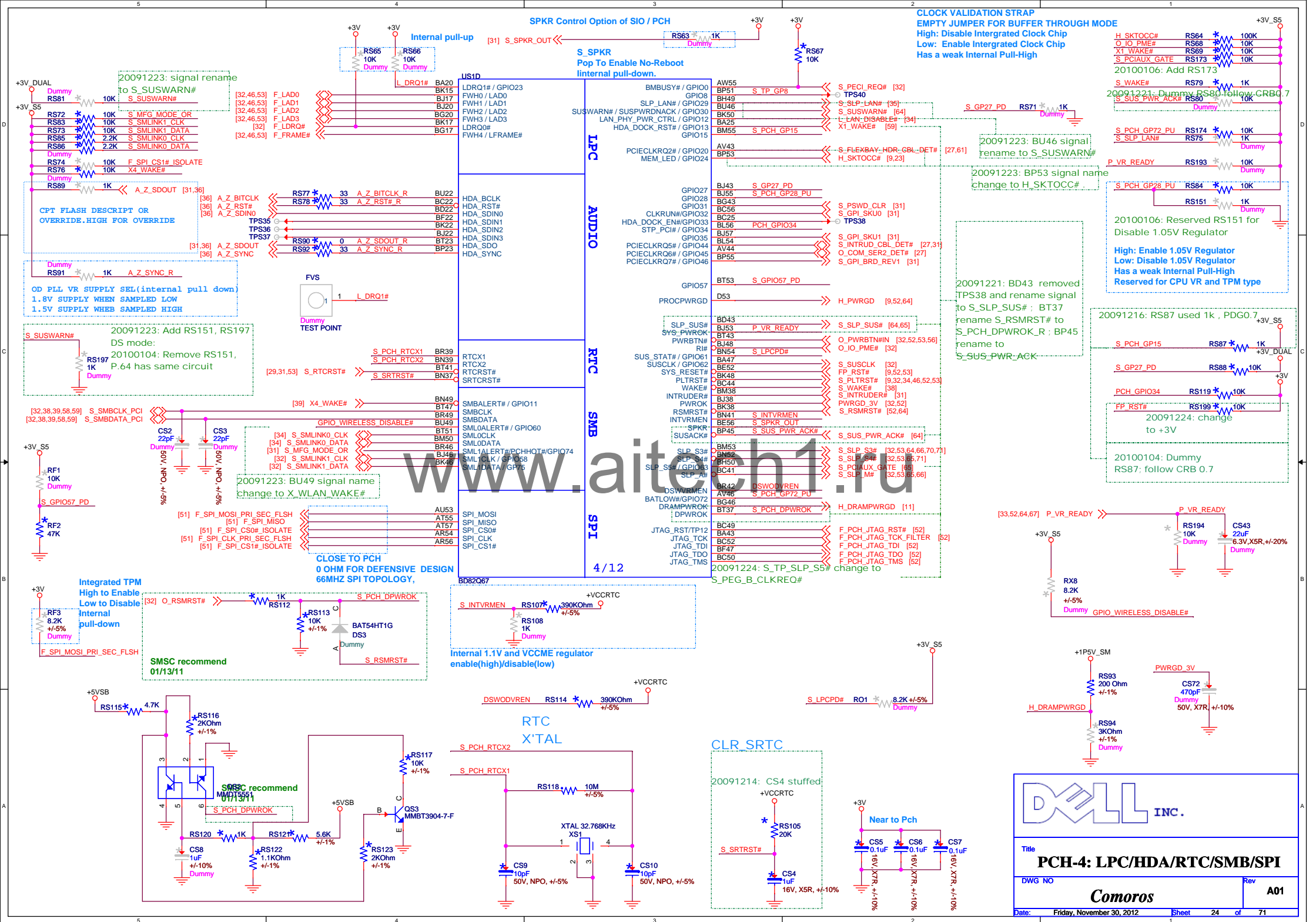
There are 4 oc pin in Controller 1 and USB 3.0 port number must be match USB 2.0, if 4*OC pin used for USB3.0, Port 4/5 will not has OC pin function can usage

Intel

PCH-2: DMI/PCIe/USB

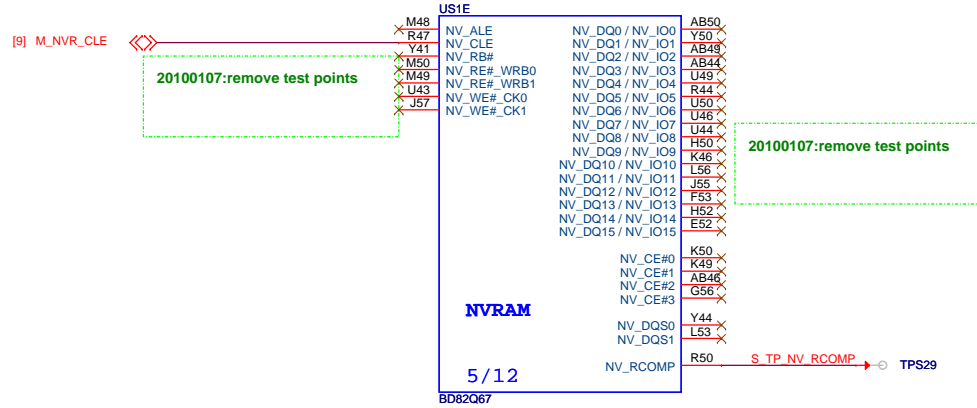
DWG NO: **Comoros** Rev: **A01**

Date: Friday, November 30, 2012 Sheet: 22 of 71

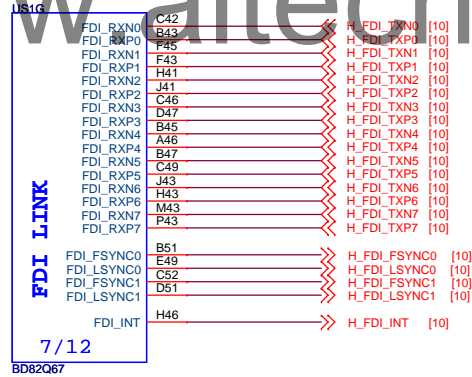



20100106: Remove ONFI function since not support

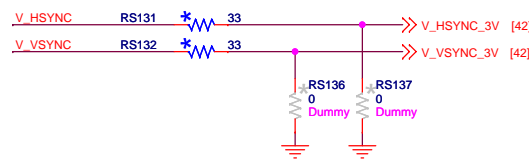
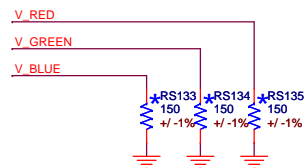
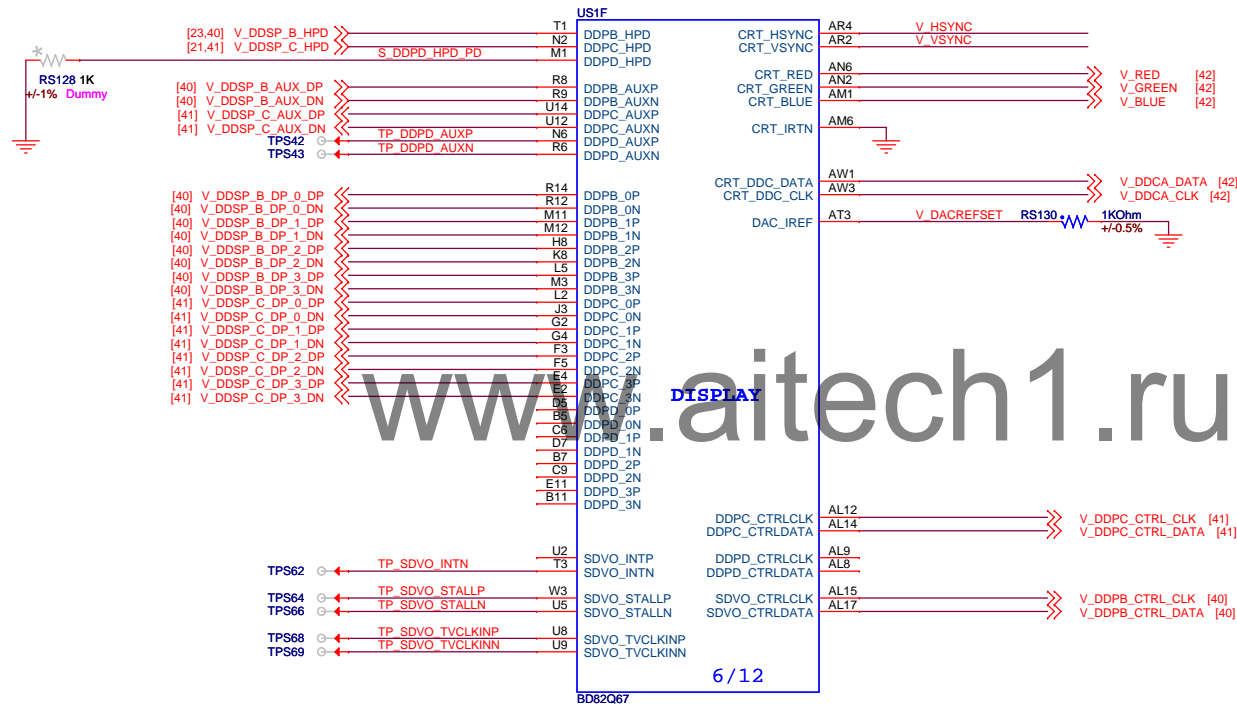
S_NVR_CLE internal pull-down.



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Title	
PCH-5/7: NVRAM/FDI	
DWG NO	Rev
Comoros	A01
Date: Friday, November 30, 2012	Sheet 25 of 71





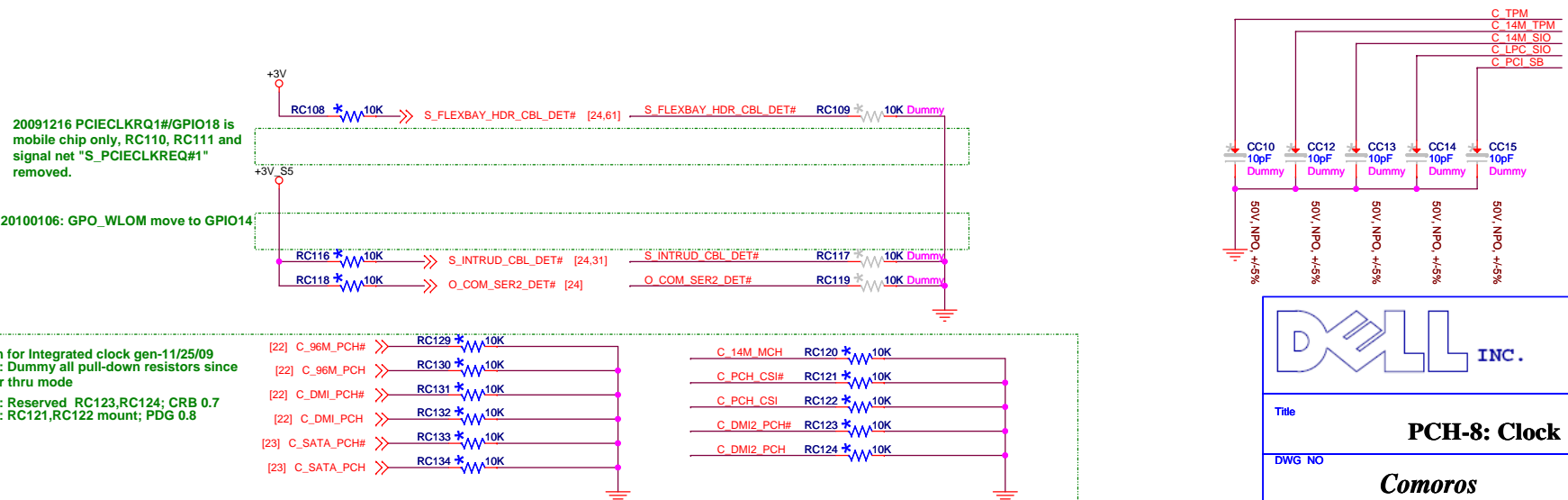
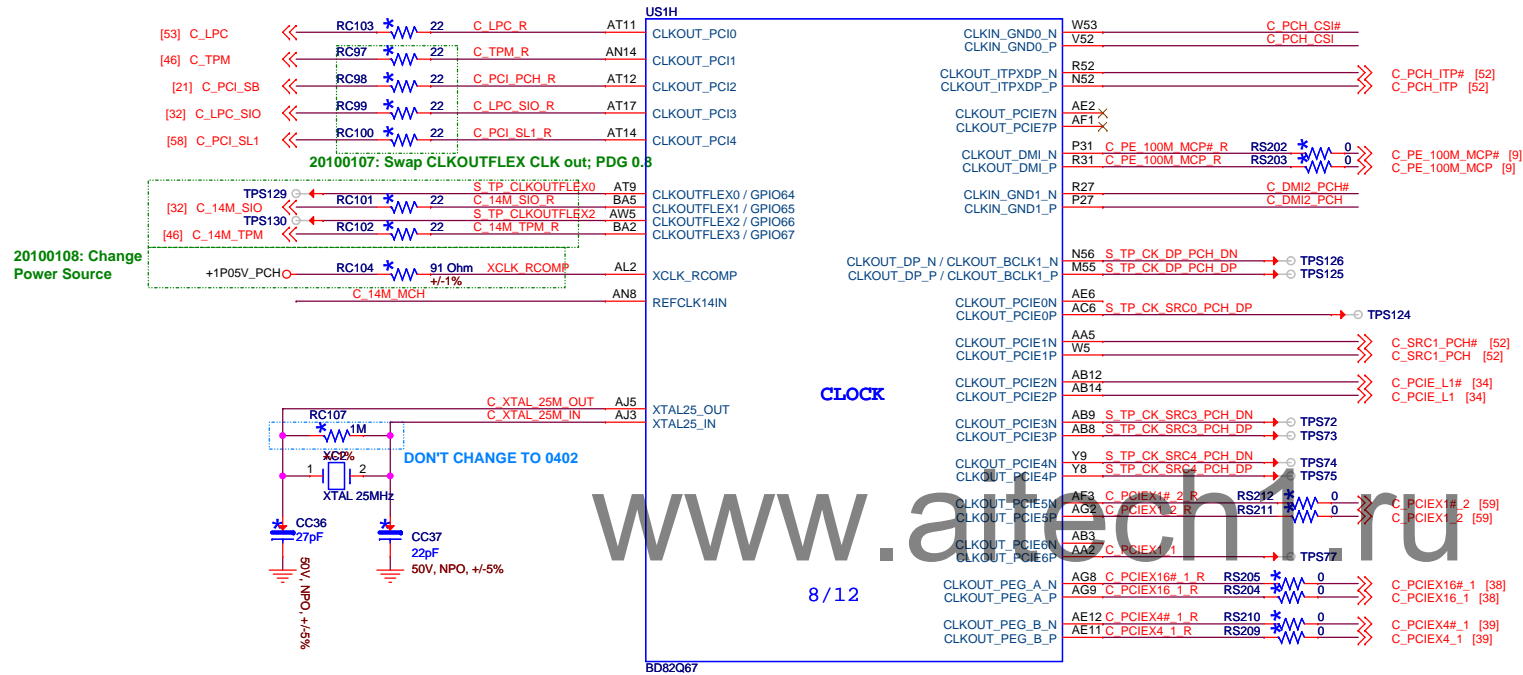
Title
PCH-6: Display

DWG NO
Comoros

Rev
A01

Date: Friday, November 30, 2012 **Sheet** 26 **of** 71

20100106: Remove RS96; CRB 0.7
20100106: Swap C_PCH_PCI0_R and C_PCI_SL1_R; CRB 0.7
20100106: Disconnect AT11 and left Test point; CRB 0.7

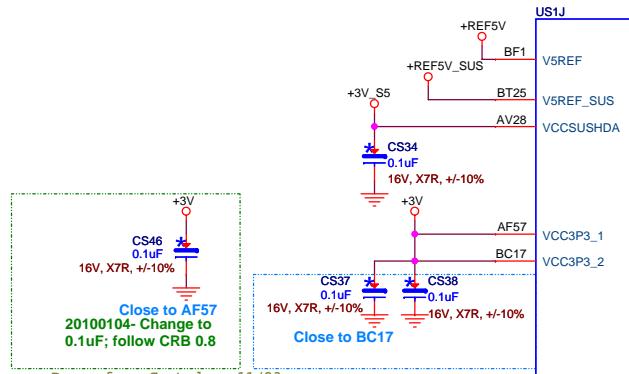


PCH-8: Clock

Comoros

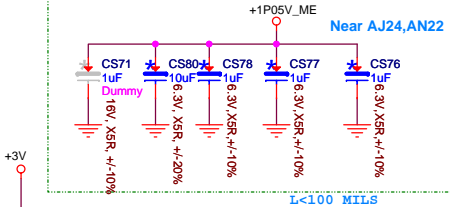
A01

Date: Friday, November 30, 2012 Sheet 27 of 71

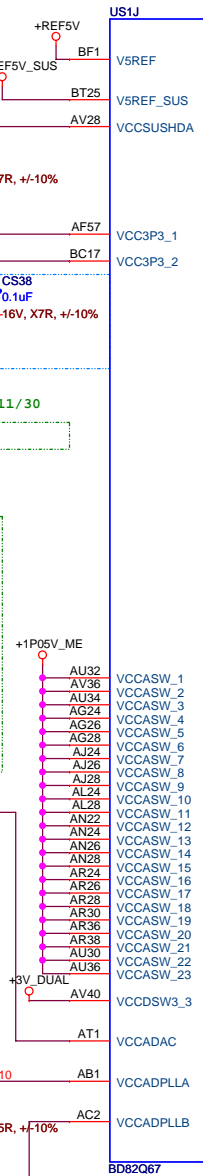
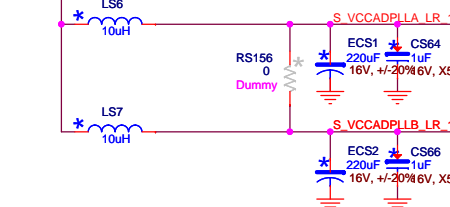
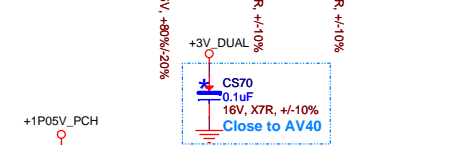


Delet LS5,RS151,CS46,CS47; follow CRB 0.7-11/30

20100104- Add CS78,CS80 and CS76,CS77 change to 0403; follow CRB 0.8



20100106:- FBS1 change to FB: PDG 0.8

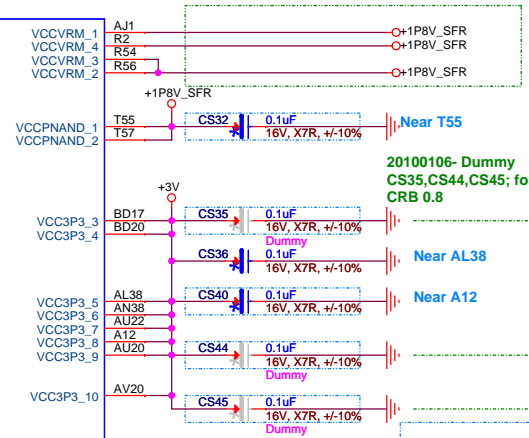


POWER

10/12

Coherent with GPIO28

Delet RS144,RS146,RS149 and 1.05V power source; follow CRB 0.7-11/30

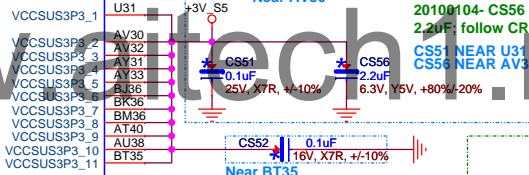


20100106- Dummy CS35,CS44,CS45; follow CRB 0.8

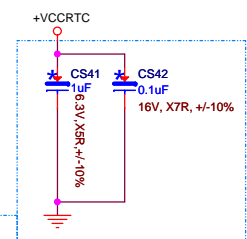
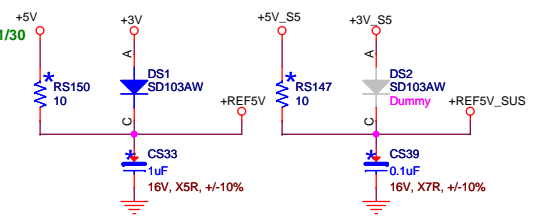
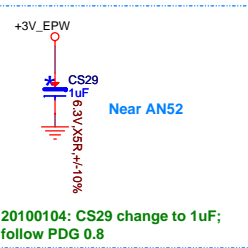
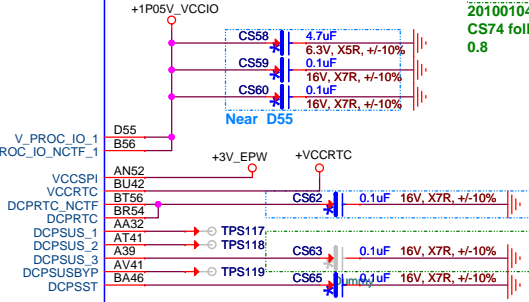
20100104- CS73,CS75 change to 1uF; follow CRB 0.8

20100104- CS56 change to 2.2uF; follow CRB 0.8

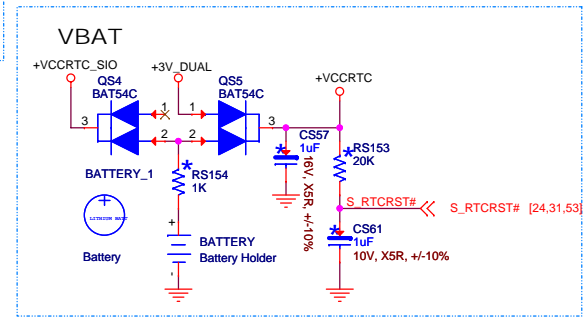
CS51 NEAR U31 CS56 NEAR AV30,AT40




20100104- Remove CS74 follow CRB 0.8



20100104- Remove CS49,CS50 follow CRB 0.8





INC.

Title

PCH-10: Power 2

DWG NO

Comoros

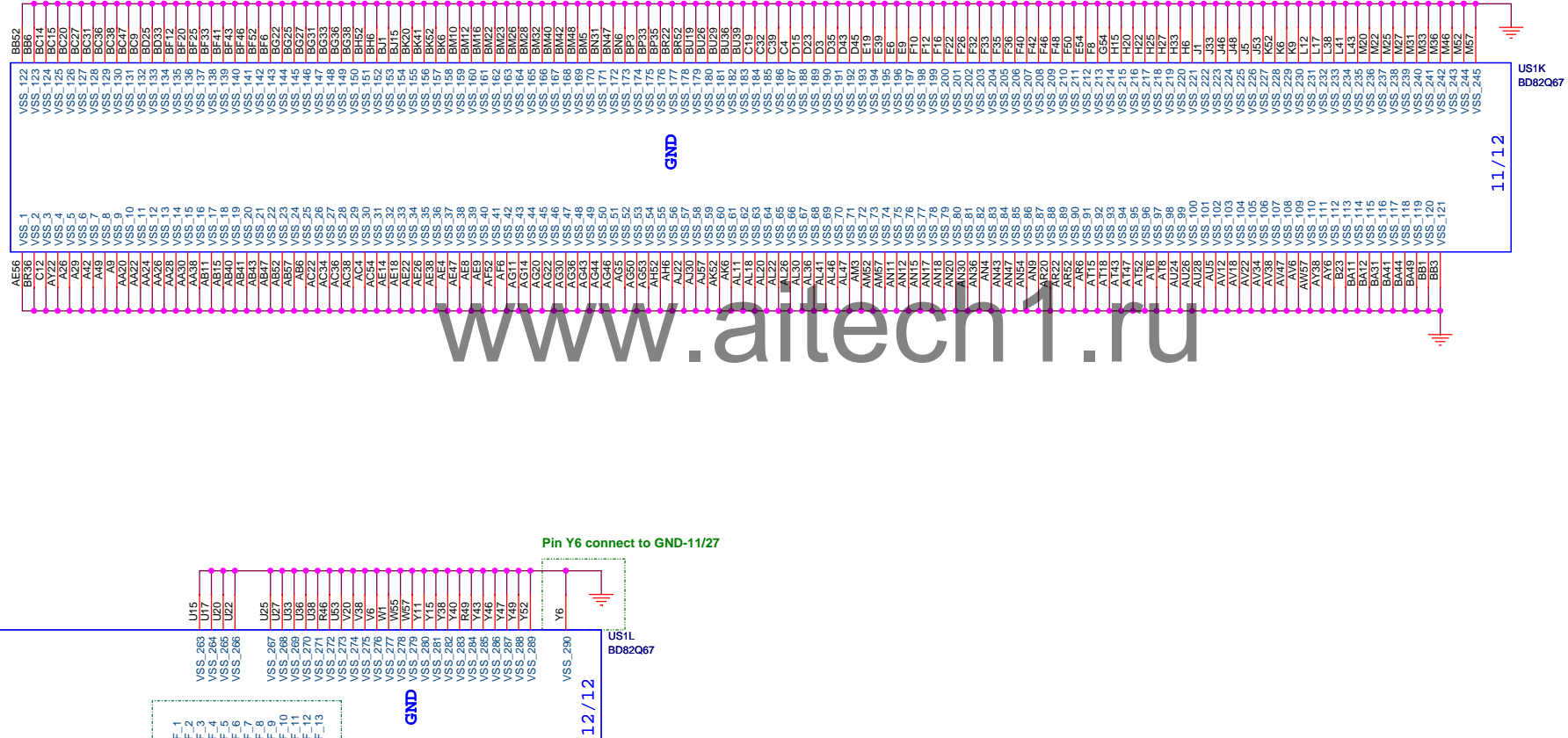
Date: Friday, November 30, 2012

Sheet 29 of 71

Rev

A01

~~By Dell request remove US1_1 PCH heatsink detect for RTCSRST net spacing~~



Title

PCH-11: GND

DWG NO	
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Comoros

Rev

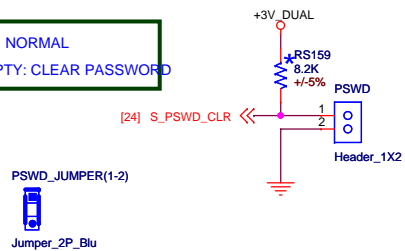
A01

Date: Friday, November 30, 2012

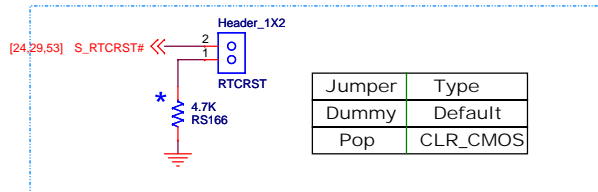
Sheet 30 of 71

Clear Password

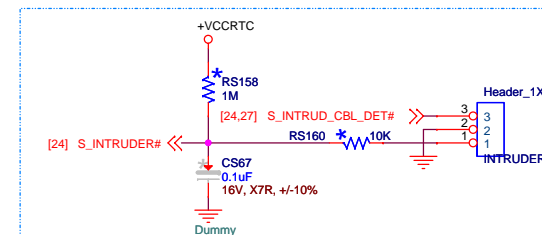
1-2: NORMAL
EMPTY: CLEAR PASSWORD



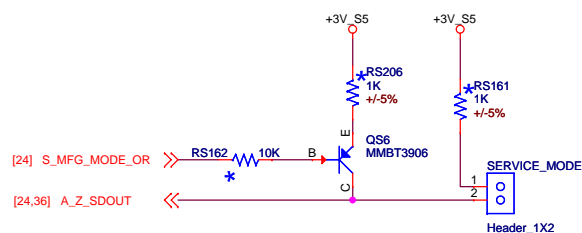
CLR_CMOS



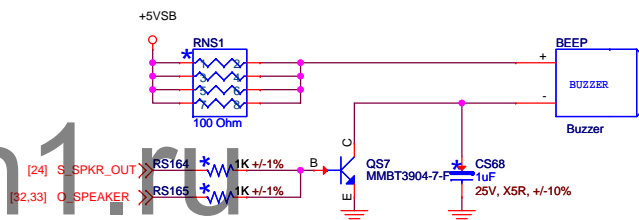
Chassis Intruder



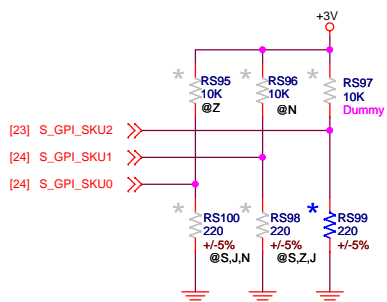
SERVICE_MODE



BEEP



SKU ID



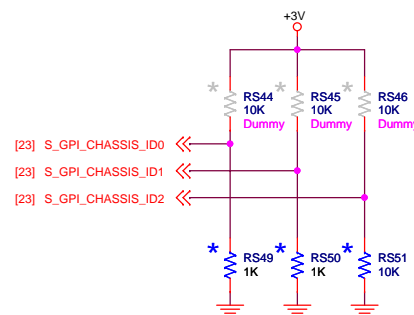
SKU ID

SKU1	SKU0	Type
0	0	TPM
0	1	TCM
1	0	non TPM/TCM
1	1	Reserved

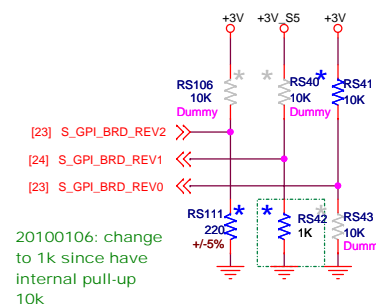
Chassis ID

check : need to update table

ID2	ID1	ID0	Type
1	0	1	SFF
1	0	0	Comoros
0	0	0	MT/DT
0	1	1	USFF



BOARD ID



Rev2	Rev1	Rev0	Type
0	0	0	A00/A01
0	0	1	A02
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved



Delet RO2; SMSC suggestion-12/08/09

Delet RO6; SMSC suggestion-12/08/09

20100107: change to +3V_DUAL for layout

Add SMBus switch
circuit-11/25/09
20100105: Mount
SMBus control
circuit by
B_ATX_PWROK

[15,16,17,18,52] S_SMBCLK_MAIN <<> S_SMBCLK_PCI [24,38,39,58,59]

[15,16,17,18,52] S_SMBDATA_MAIN <<> S_SMBDATA_PCI [24,38,39,58,59]

20100111:
Remove PSU
PWM control

DO1 change to RO109; SMSC suggestion-12/08/09

Delet RO36,RO37 and connect Tmin_Shift to PCH directly; SMSC suggestion-12/08/09

RO20 8.2K +/-5% O_AUD_PCSKPR_DET#
RO21 8.2K +/-5% O_BC_CLK
RO22 8.2K +/-5% SPI_DI
RO38 100K +/-5% T_ESATA_DET#
RO24 4.7K +/-5% S_SMBDATA_MAIN
RO25 4.7K +/-5% S_SMBCLK_MAIN
RO26 30K +/-1% O_TXD1_R
RO27 8.2K +/-5% TMIN_SHIFT

RO13 4.7K +/-5% S_SMBDATA_PCI
RO14 4.7K +/-5% S_SMBCLK_PCI

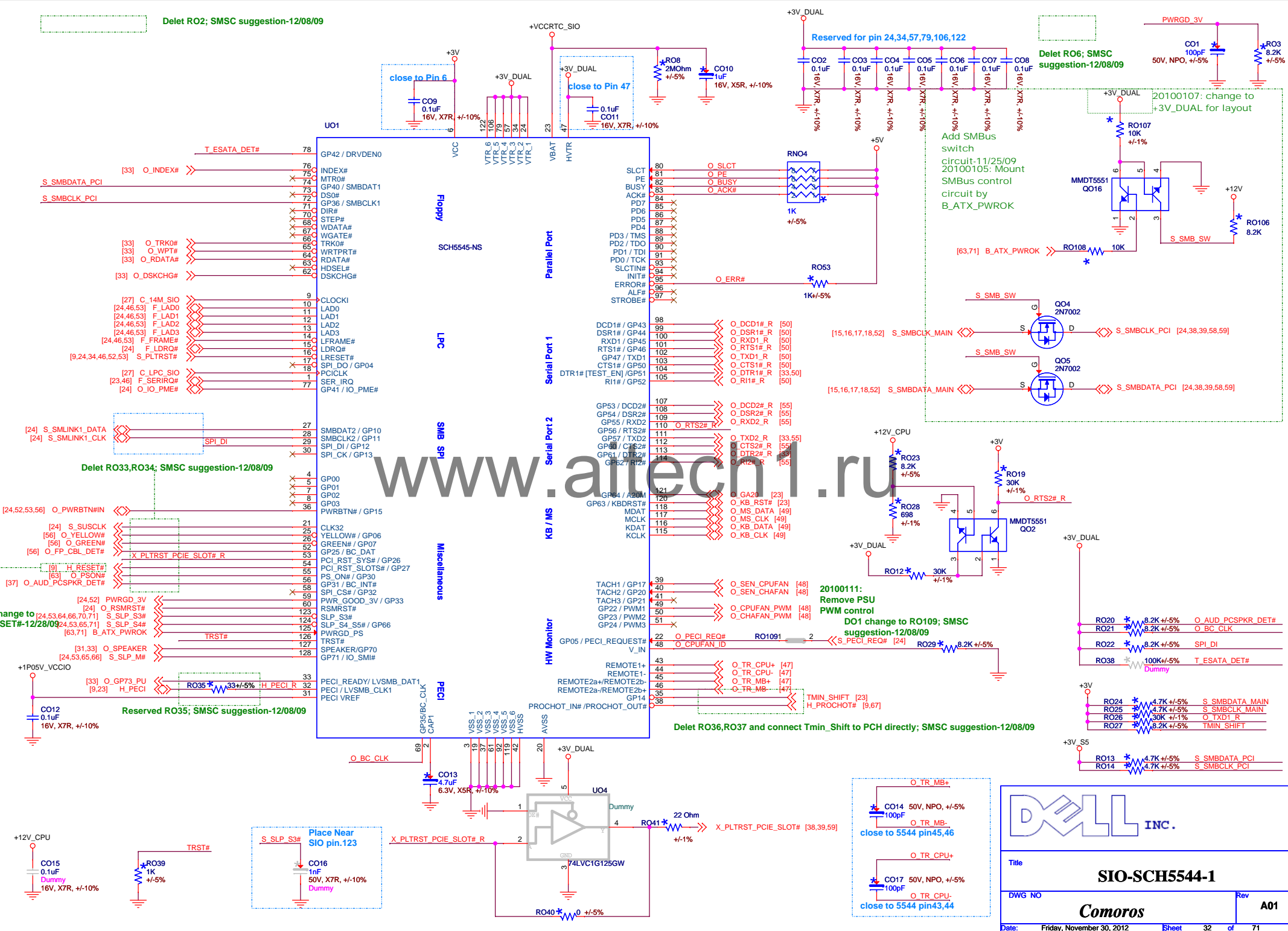
DELL INC.

Title: **SIO-SCH5544-1**

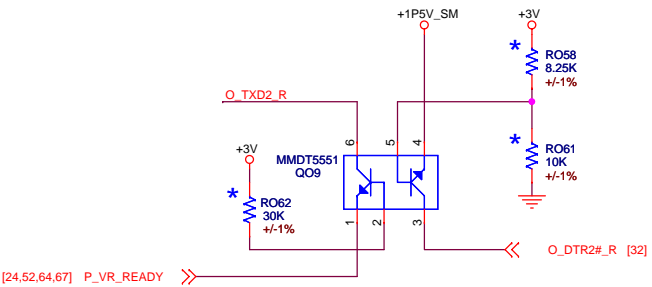
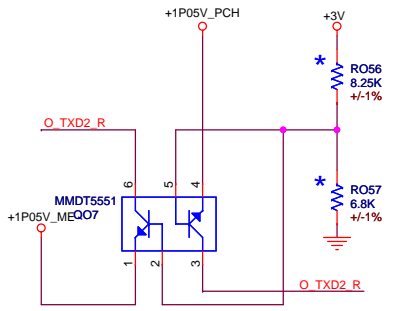
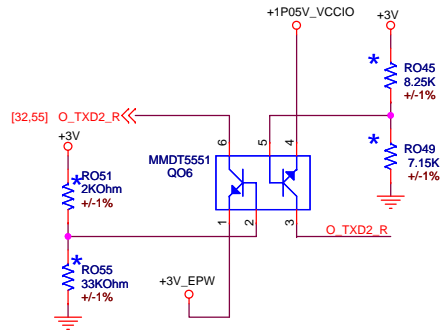
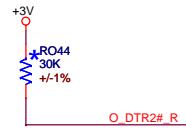
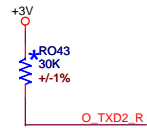
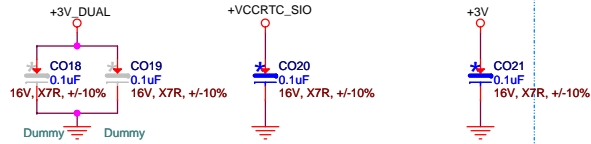
DWG NO: **Comoros** Rev: **A01**

Date: Friday, November 30, 2012 Sheet: 32 of 71

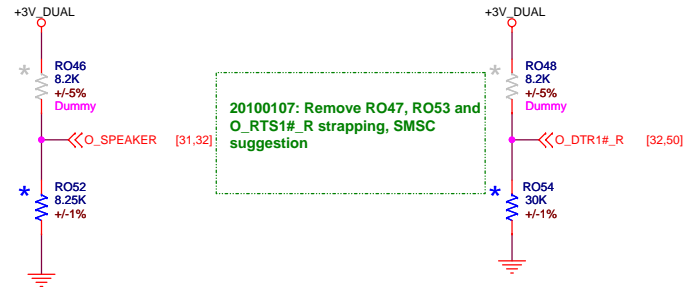
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SCH5544 Decoupling



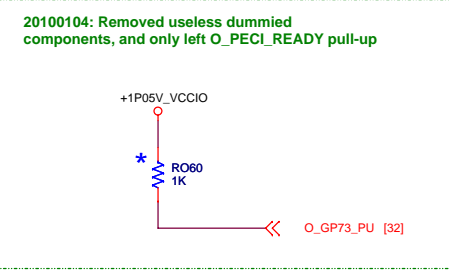
5544 PRE-POST DIAG PG GENERATION



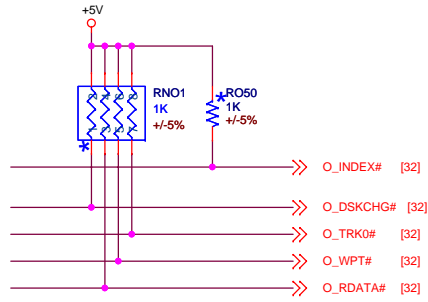
20100107: Remove RO47, RO53 and O_RTS1#_R strapping, SMSC suggestion

	SPEAKER	DTR1#
	Diag_En	Flash_en
PULL HIGH	Disable	Flash Enable
PULL LOW	Enable	Parallel Enable

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20100104: Removed useless dummied components, and only left O_PECI_READY pull-up



Title

SIO-SCH5544-2 (MISC)

DWG NO

Comoros

Date: Friday, November 30, 2012

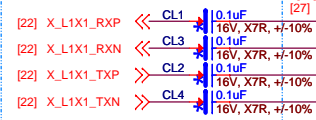
Rev

A01

Sheet 33 of 71

20091216 Intel 82579 schematic check list 0.5:
Change net name from CLK_REQ_N to S_FLEXBAY_HDR_CBL_DET#
20100105: Remove RL2 and S_FLEXBAY_HDR_CBL_DET#
connection since useless; PDG 0.8

near the PCIe transmitter.



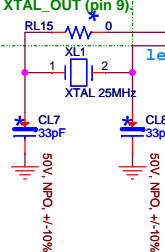
[24] S_SMLINK0_CLK
[24] S_SMLINK0_DATA

L LAN_DISABLE#

[35] L_ACTLEDN
[35] L_LINK100#
[35] L_LINK10#

ALWAYS DUMMY

20091216 CRB0.7 :Connect a series CL24 (10 pF) capacitor to XTAL_OUT (pin 9).



less than 325 mils

L LAN_TESTEN

TEST_ENABLE

RBIAS

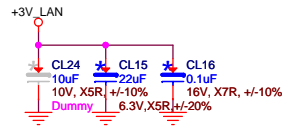
21040FE00-187-G

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Net VDD1P0 and L1_LAN_1P0_CTRL keep short and wide

20100107: Dummy RL9 and Mount LL1; CRB 0.7

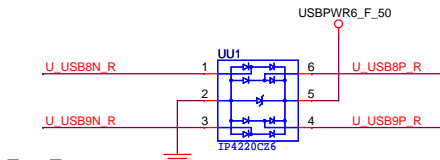
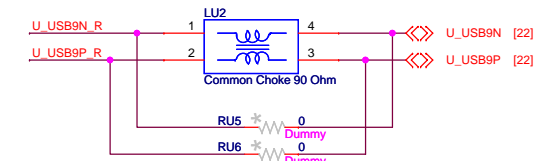
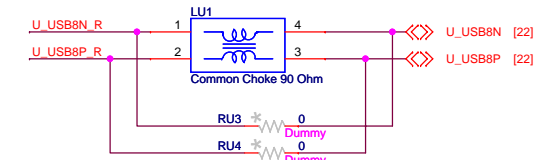
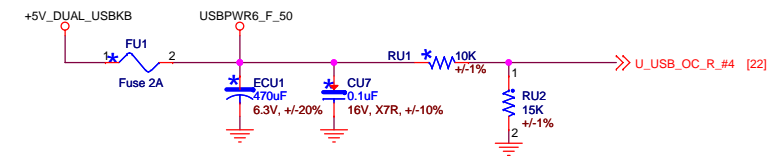
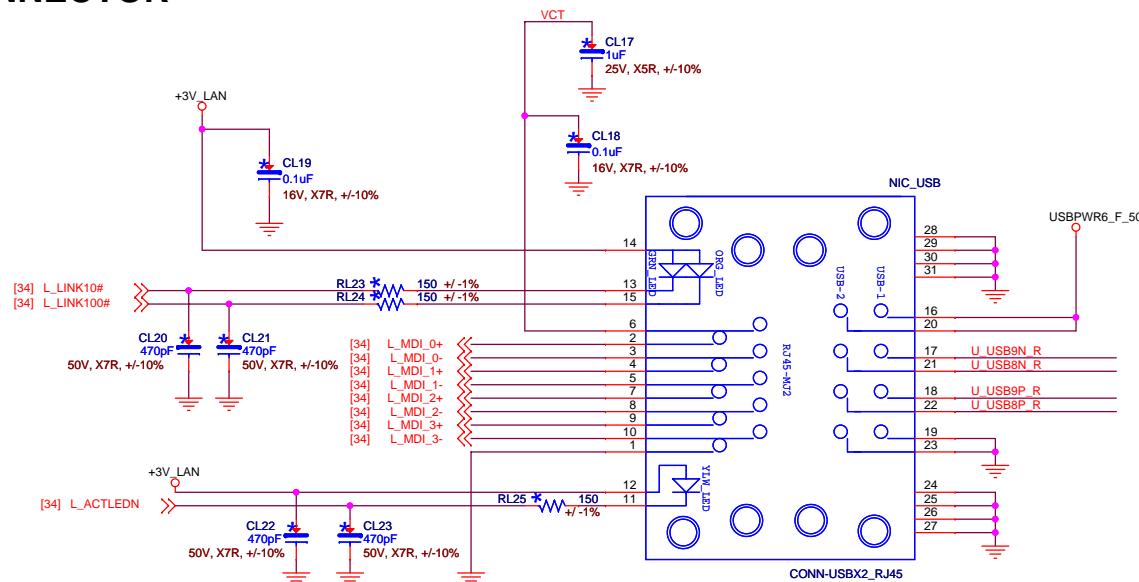
Close to PIN5 (VDD)



20091216 follow CRB0.7 and 82579 checklist: does not require any MDI termination.(delete => RL15, RL16, RL17, RL18, RL19, RL20, RL21, RL22, CL11, CL12, CL13, CL14)

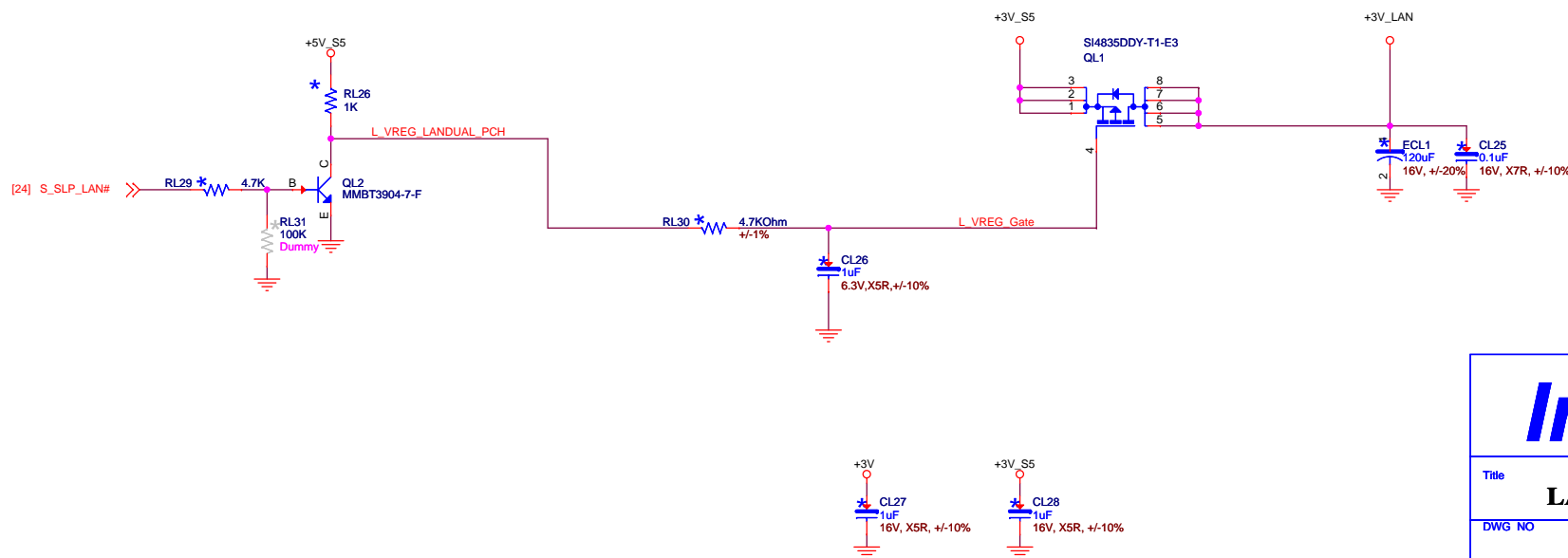


LAN CONNECTOR



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LAN POWER

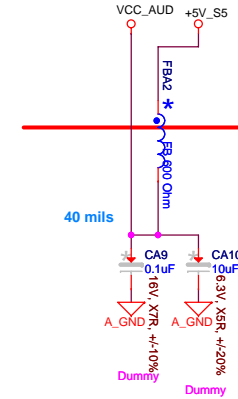
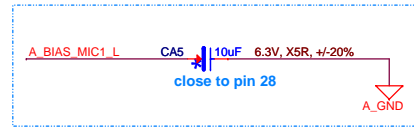
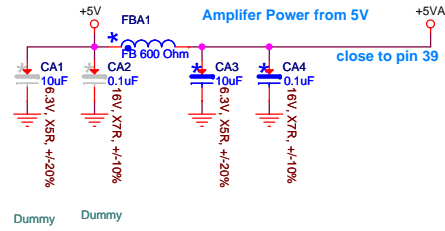


Intel

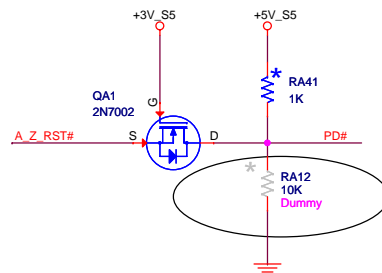
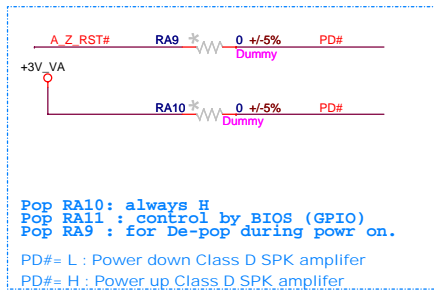
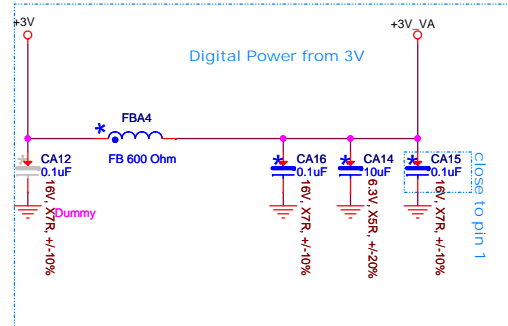
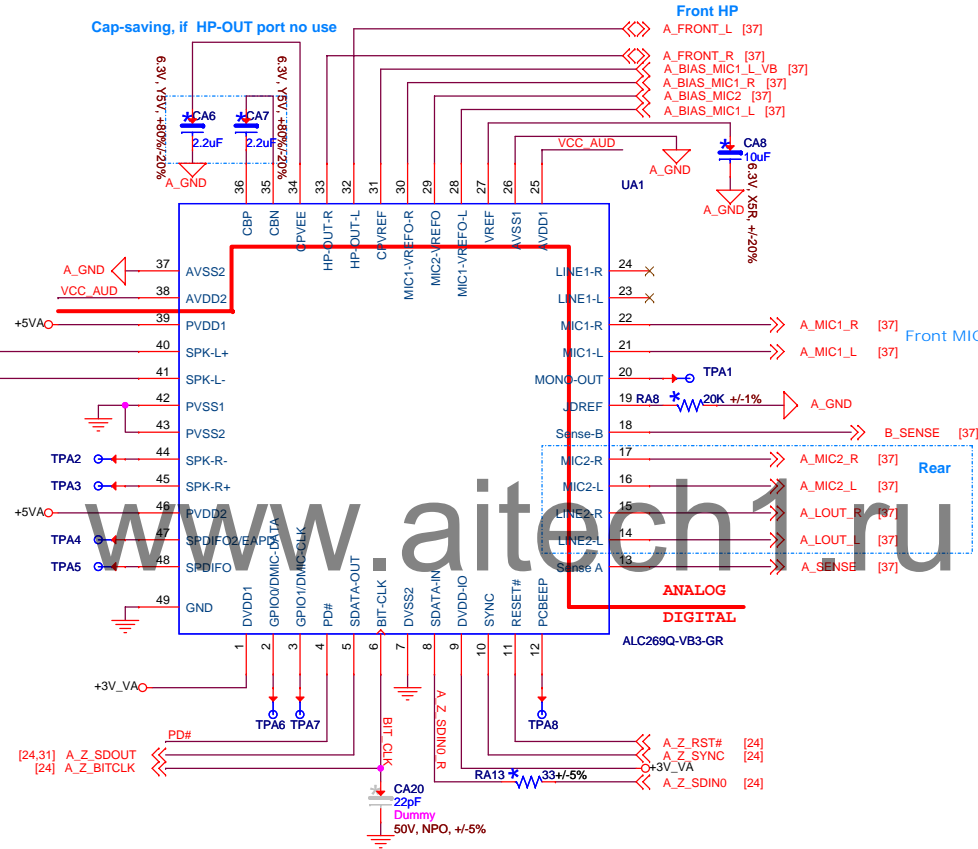
Title LAN Power & LAN/USB Conn

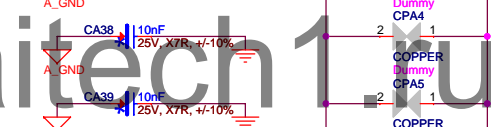
DWG NO Comoros Rev A01

Date: Friday, November 30, 2012 Sheet 35 of 71



Cap-saving, if HP-OUT port no use



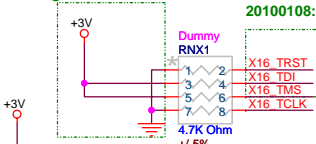


			
Title			
<h1 style="text-align: center;">Audio Conn</h1>			
DWG NO <h2 style="text-align: center;">Comoros</h2>			Rev <h2 style="text-align: center;">A01</h2>
Date:	Friday, November 30, 2012	Sheet	37 of 71

20100513: RNX1 pin1 change
connection to GND and pin5
change connection to +3V

20100108: Swap pin for layout

2010317: Slot1 change to Blue,
Foxconn P/N: 34030EK00-600-G



X_1X16_RXP[15..0] [10]
X_1X16_RXN[15..0] [10]

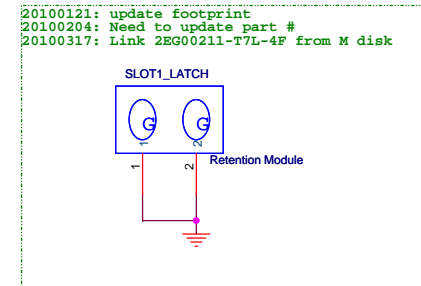
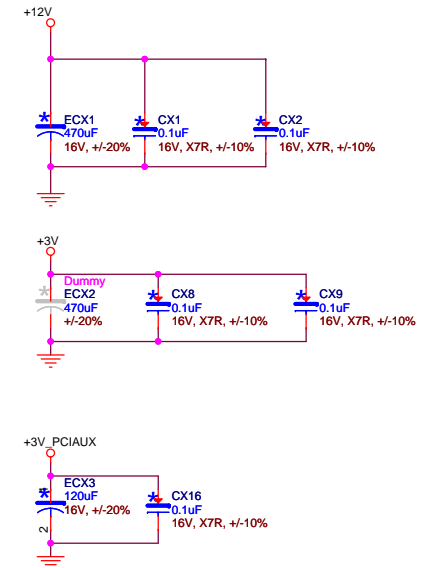
[10] X_1X16_TXP[15..0] >>
[10] X_1X16_TXN[15..0] >>

[24,32,39,58,59] S_SMBCLK_PCI
[24,32,39,58,59] S_SMBDATA_PCI

[24] S_WAKE# <<

X_PLTRST_PCIE_SLOT# [32,39,59]

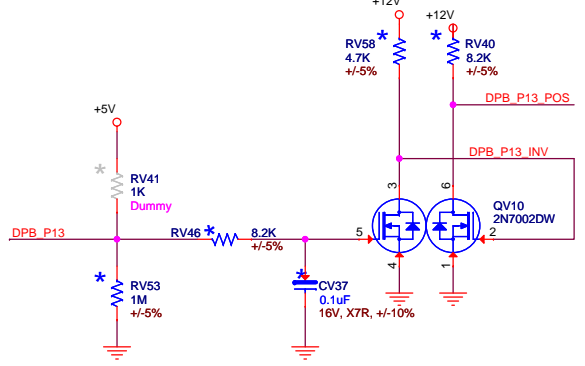
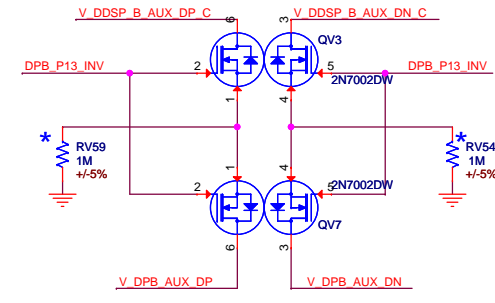
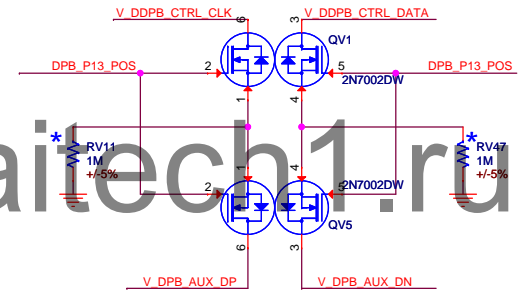
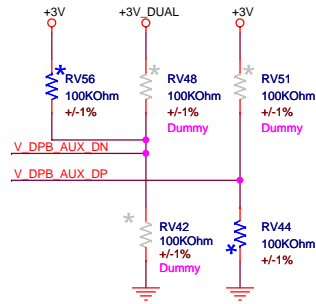
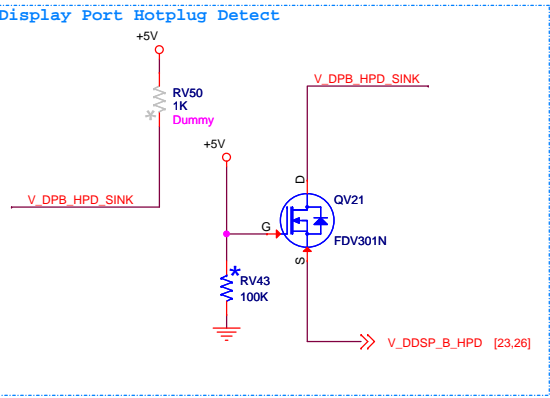
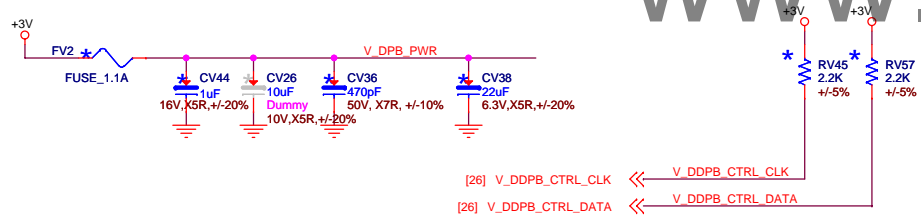
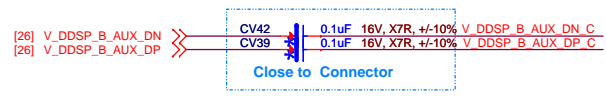
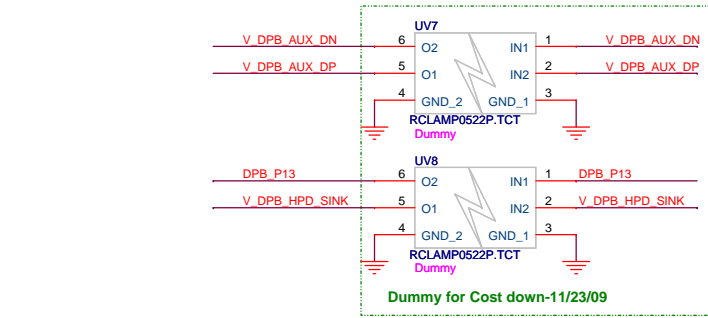
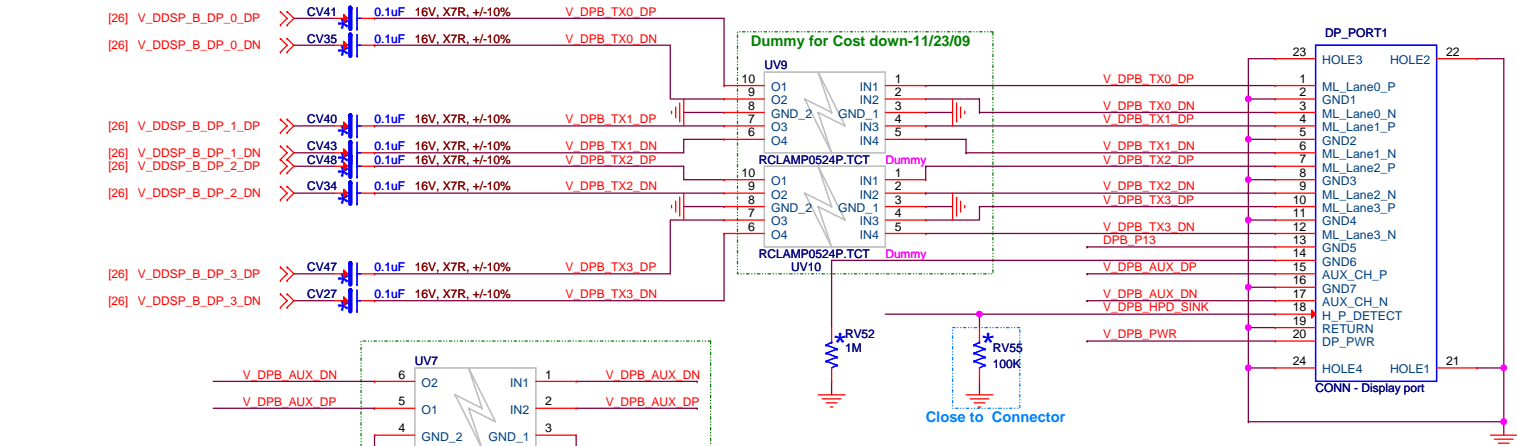
C_PCIE16_1 [27]
C_PCIE16#_1 [27]



20100121: update footprint
20100204: Need to update part #
20100317: Link 2EG00211-T7L-4F from M disk

Title Slot1: PCIe 16x	
DWG NO Comoros	Rev A01
Date: Friday, November 30, 2012	Sheet 38 of 71

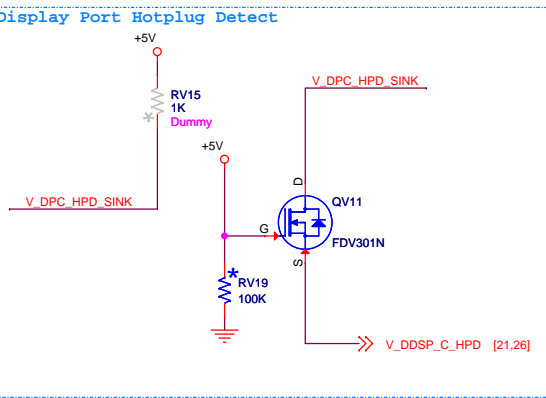
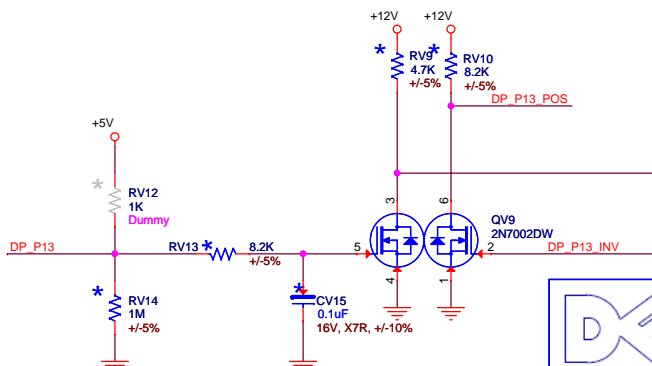
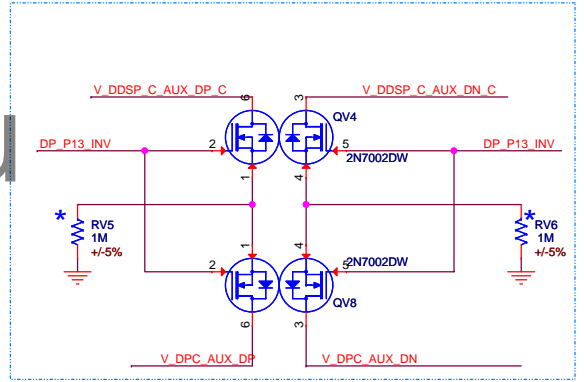
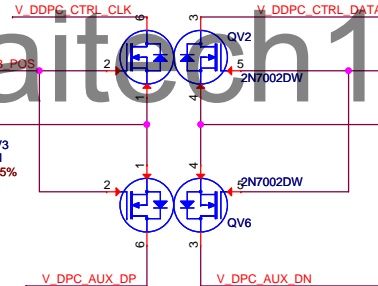
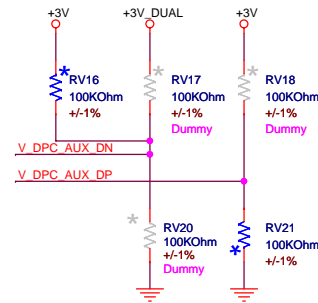
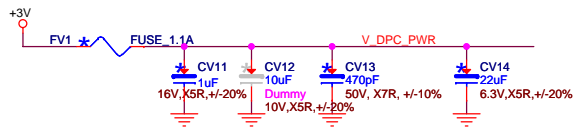
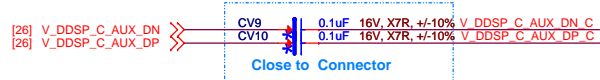
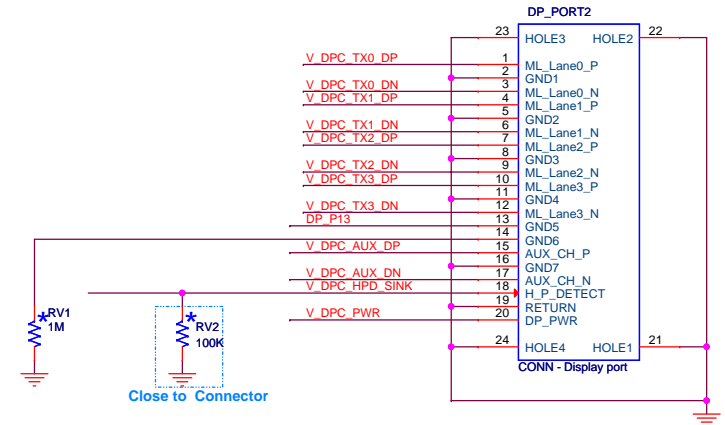
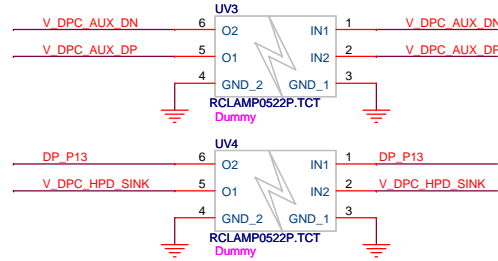
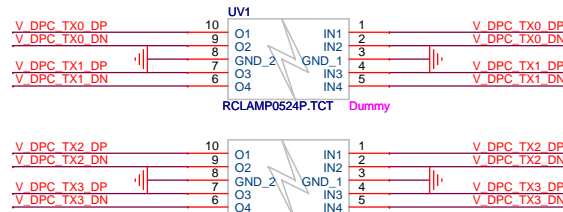
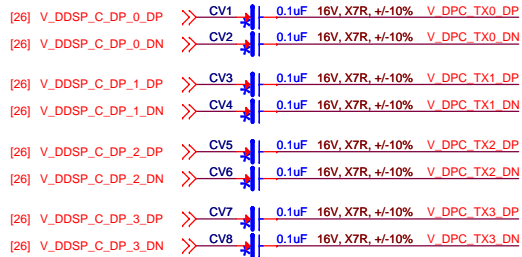
340303U00-600-G
340304R00-278-G
340304J00-317-G
340306Y00-GRS-G



DVI-D+VGA Conn

DWG NO **Comoros** Rev **A01**

Date: Friday, November 30, 2012 Sheet 40 of 71



DELL INC.

Title

Display Port

DWG NO

Comoros

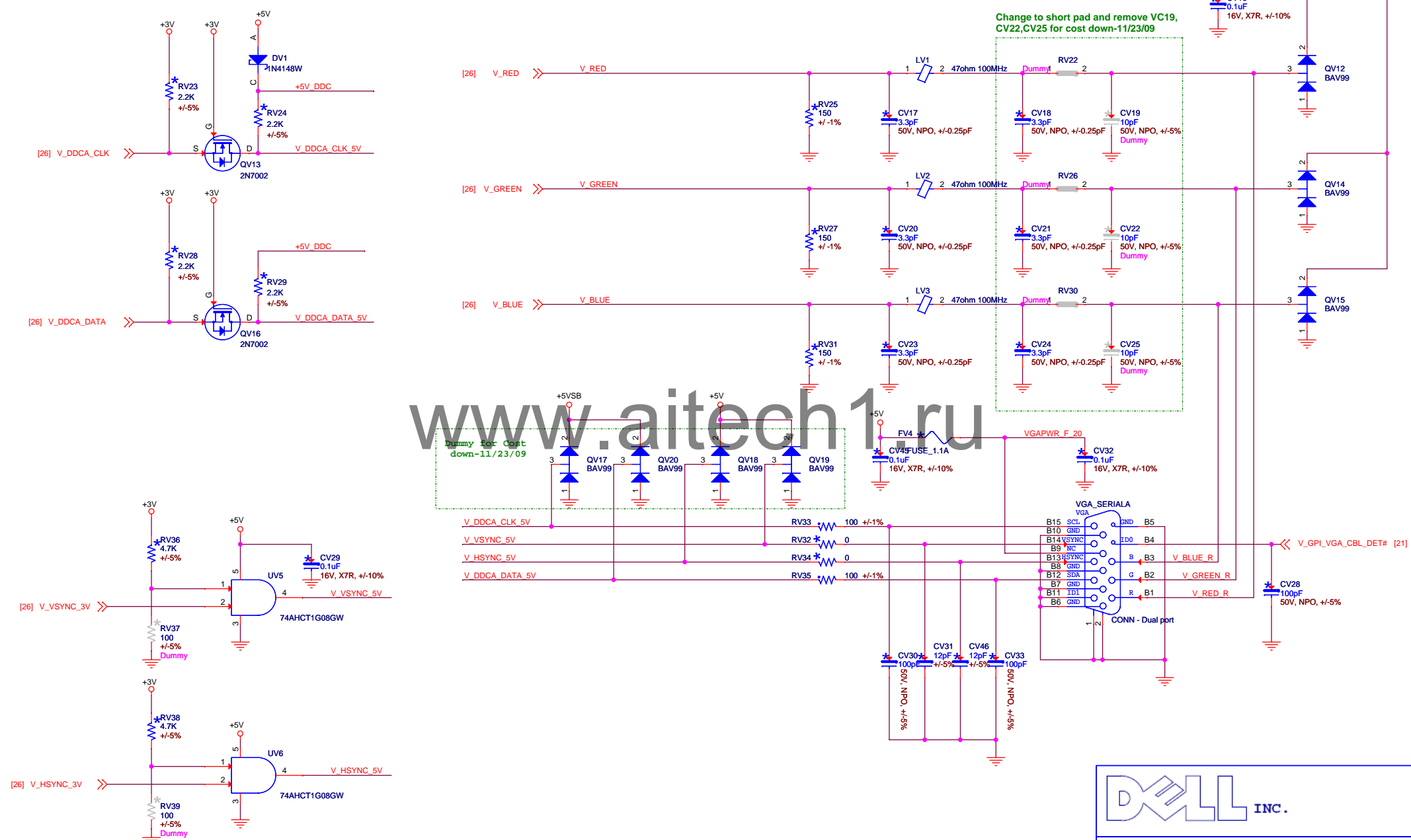
Rev

A01

Date: Friday, November 30, 2012

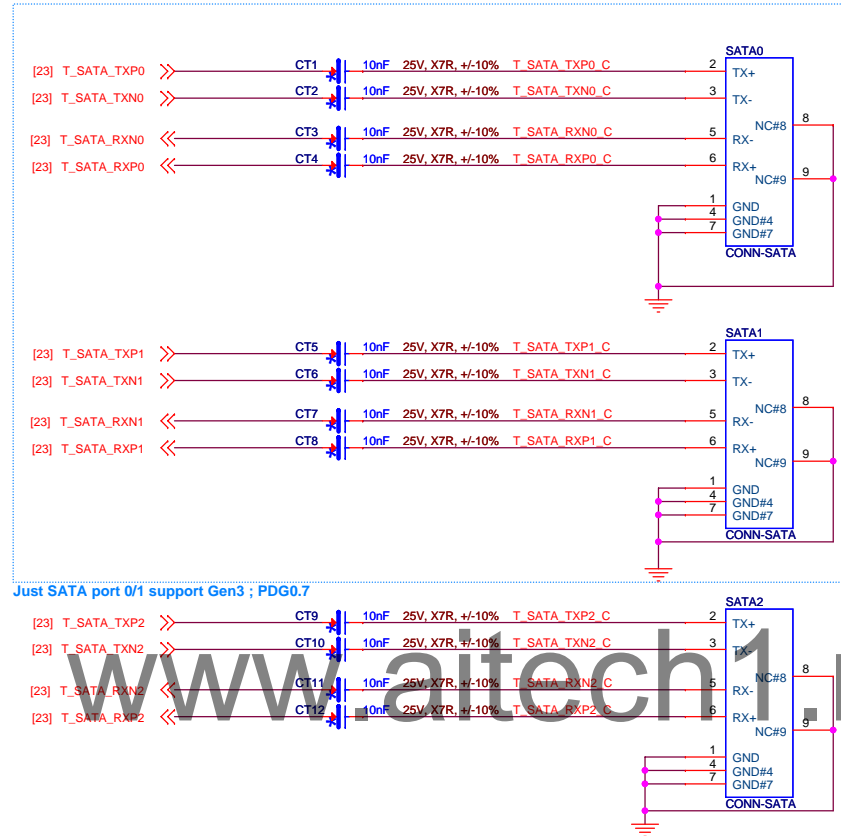
Sheet 41 of 71

VGA Connector



Title		VGA Conn	
DWG NO	Comoros	Rev	A01
Date:	Friday, November 30, 2012	Sheet	42 of 71

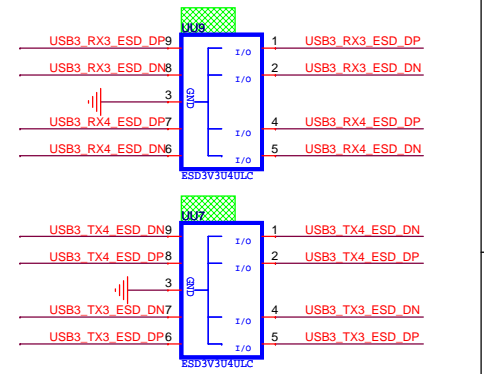
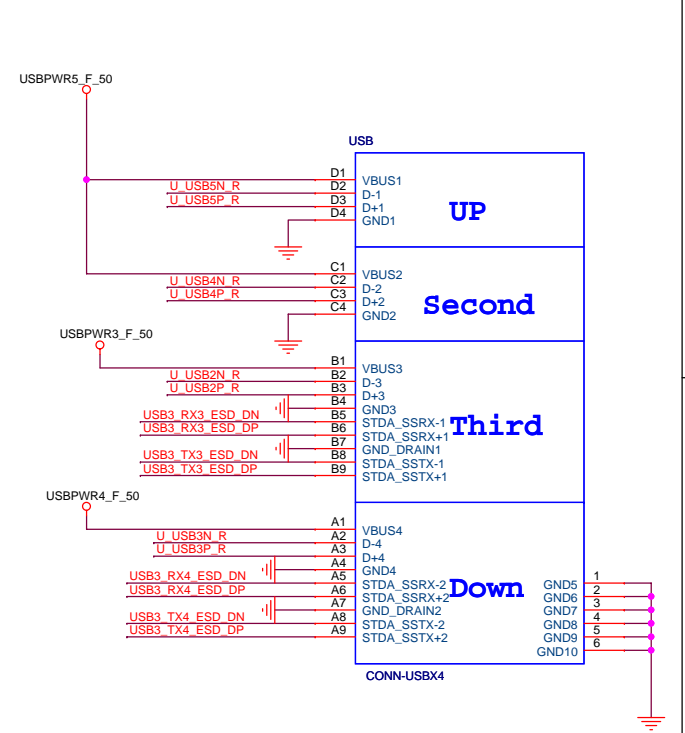
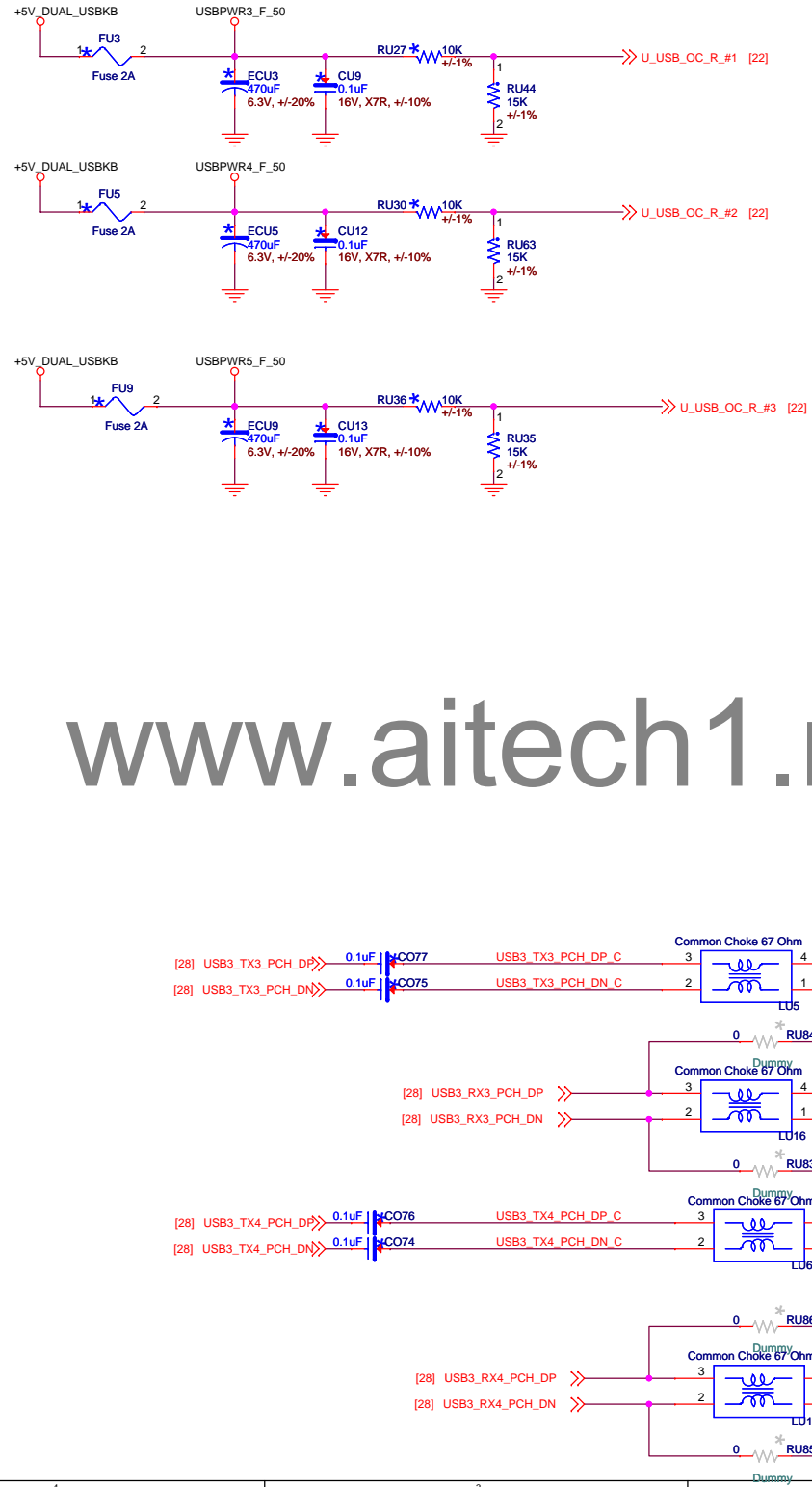
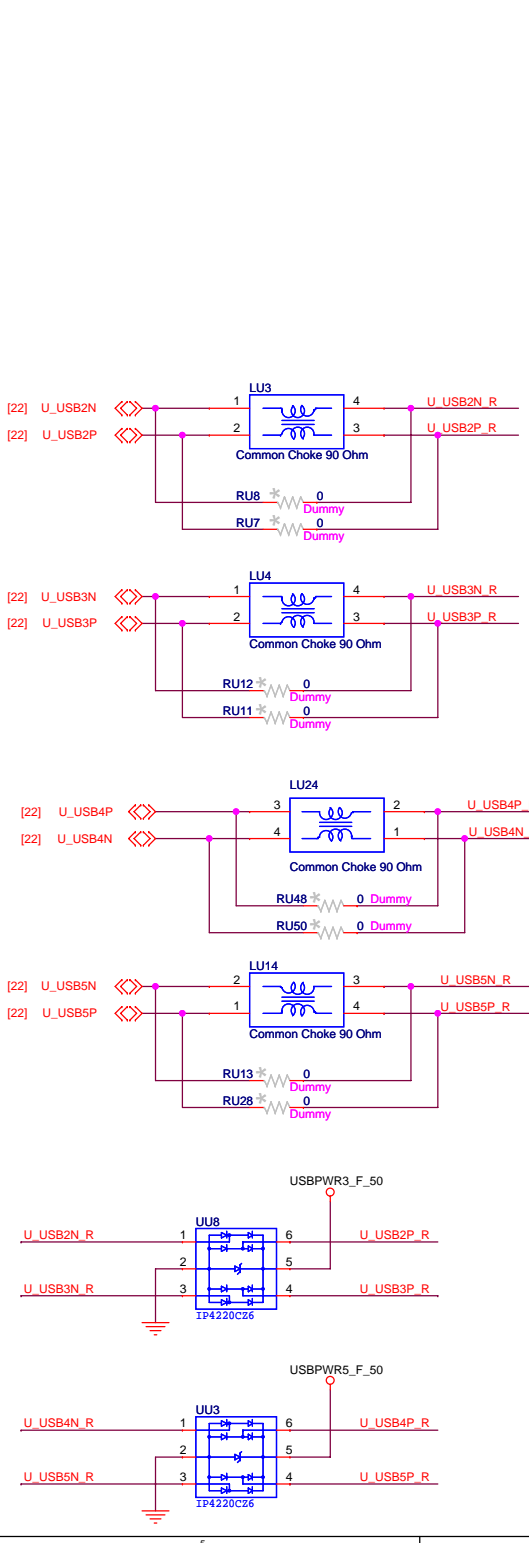
SATA x 3



DELL INC.	
Title	
SATA Conn	
DWG NO	Rev
Comoros	A01
Date: Friday, November 30, 2012	Sheet 43 of 71

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Title TBD		
DWG NO Comoros	Rev A01	
Date: Friday, November 30, 2012	Sheet 44 of 71	1



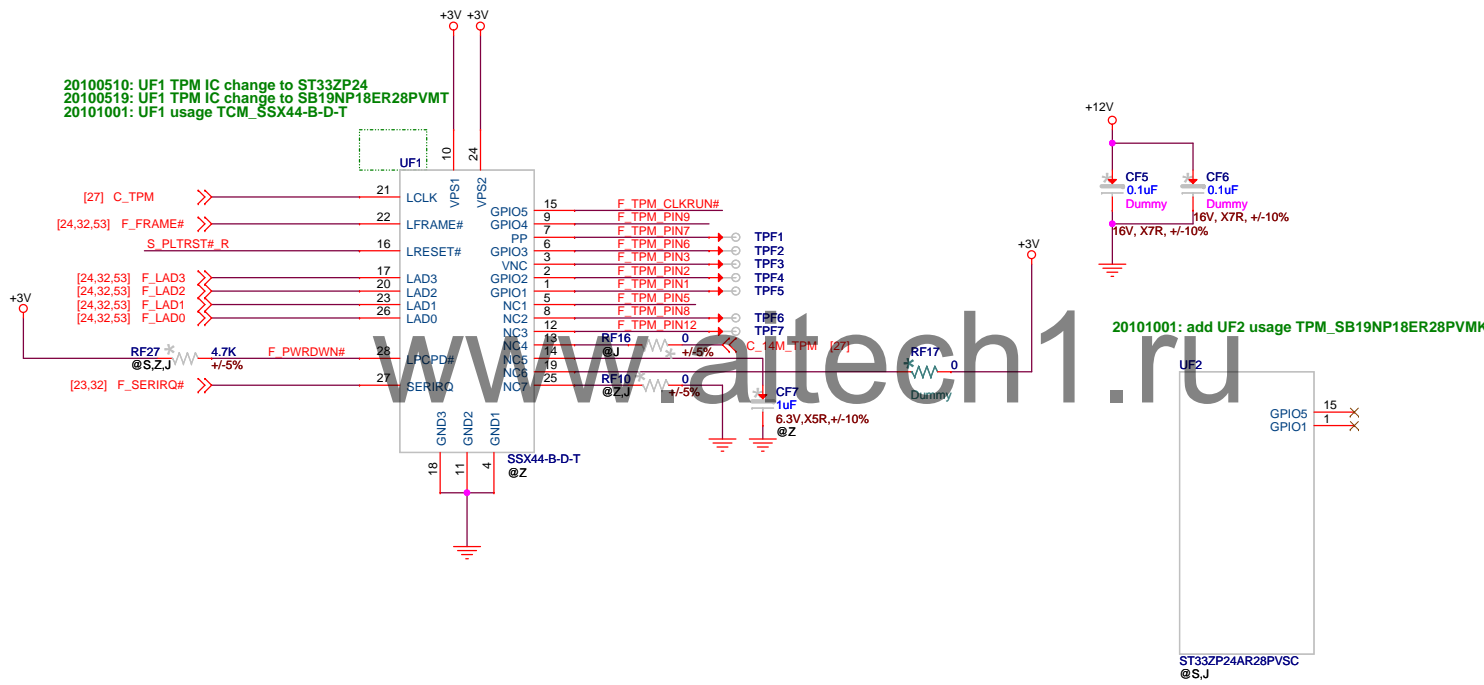
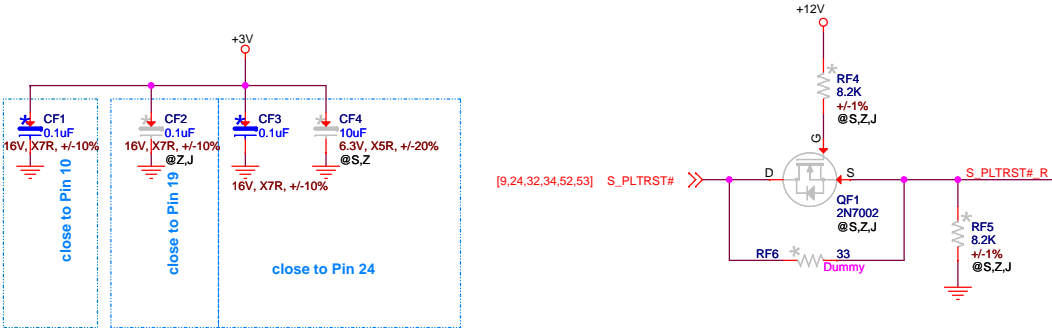
Rear USB

DWG NO **Comoros** Rev **A01**

Date: Friday, November 30, 2012 Sheet 45 of 71

TPM, TCM (TCM is just reserved because MRD has removed TCM requirement)

(Default) ST Micro	POP S	CF4
ZTE	POP Z	CF2,CF4,CF7,RF10,RF19,RF20,RF21
Jetway	POP J	CF2,CF8,RF10,RF16,RF21



Title

TPM & TCM

DWG NO

Comoros

Rev

A01

Date:

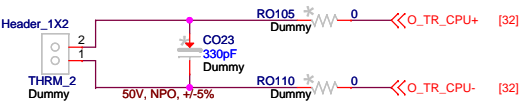
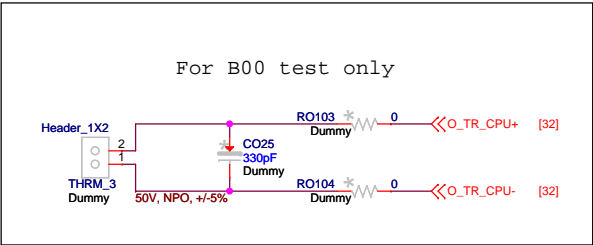
Friday, November 30, 2012

Sheet

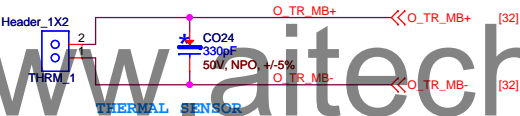
46

of

71

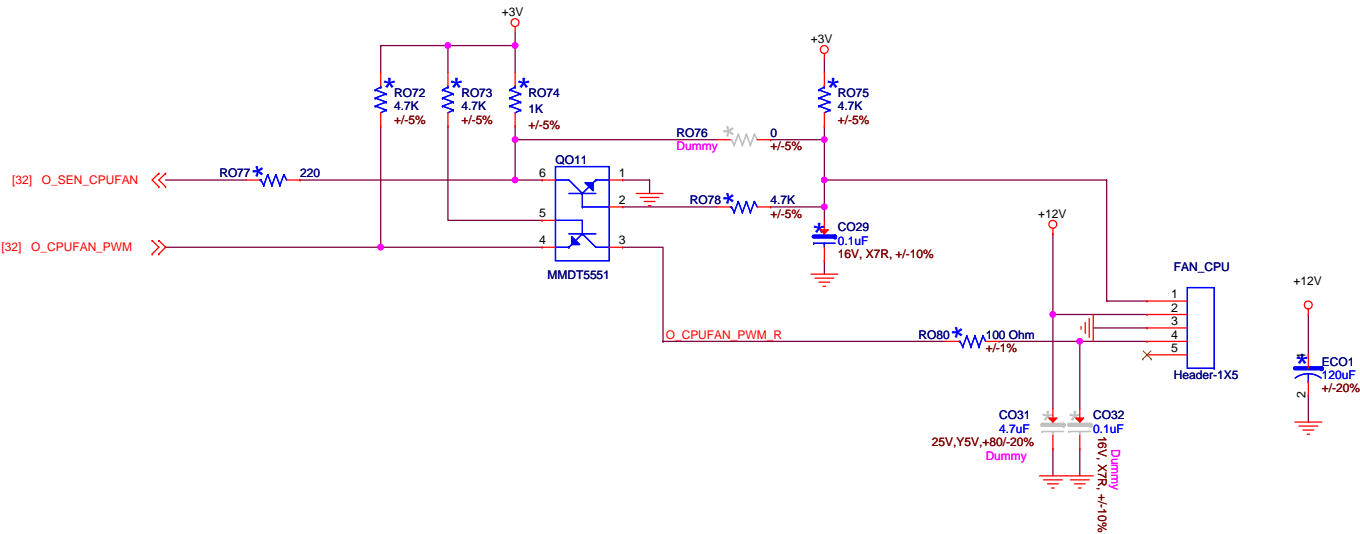


Dummy THRM2,CO23; ME suggestion-12/04/09

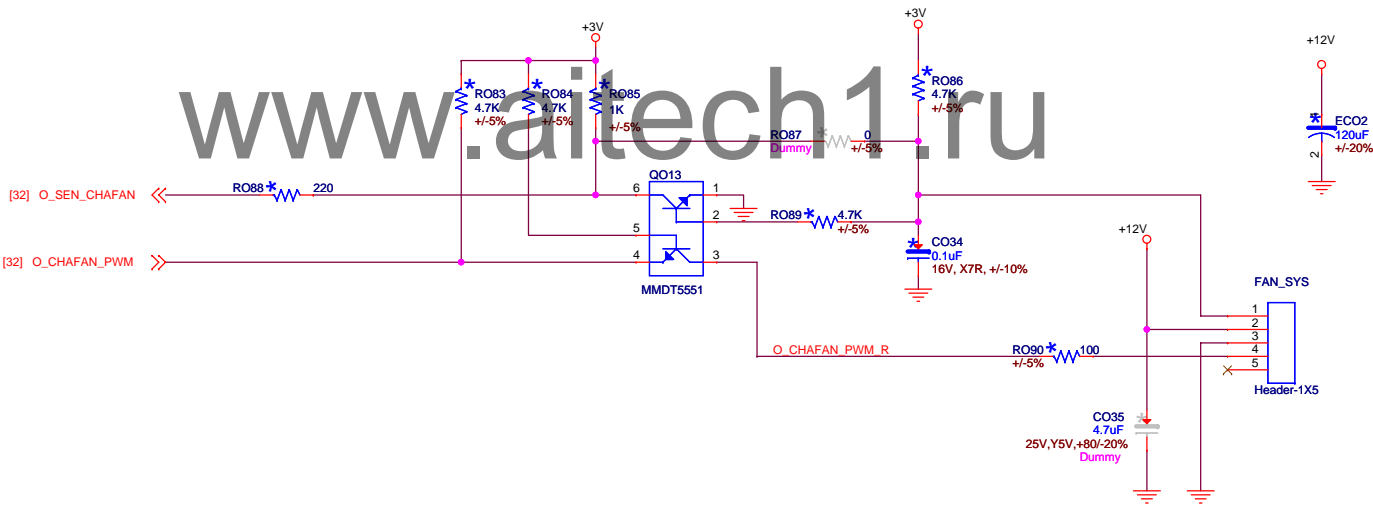


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CPU Fan



SYS Fan



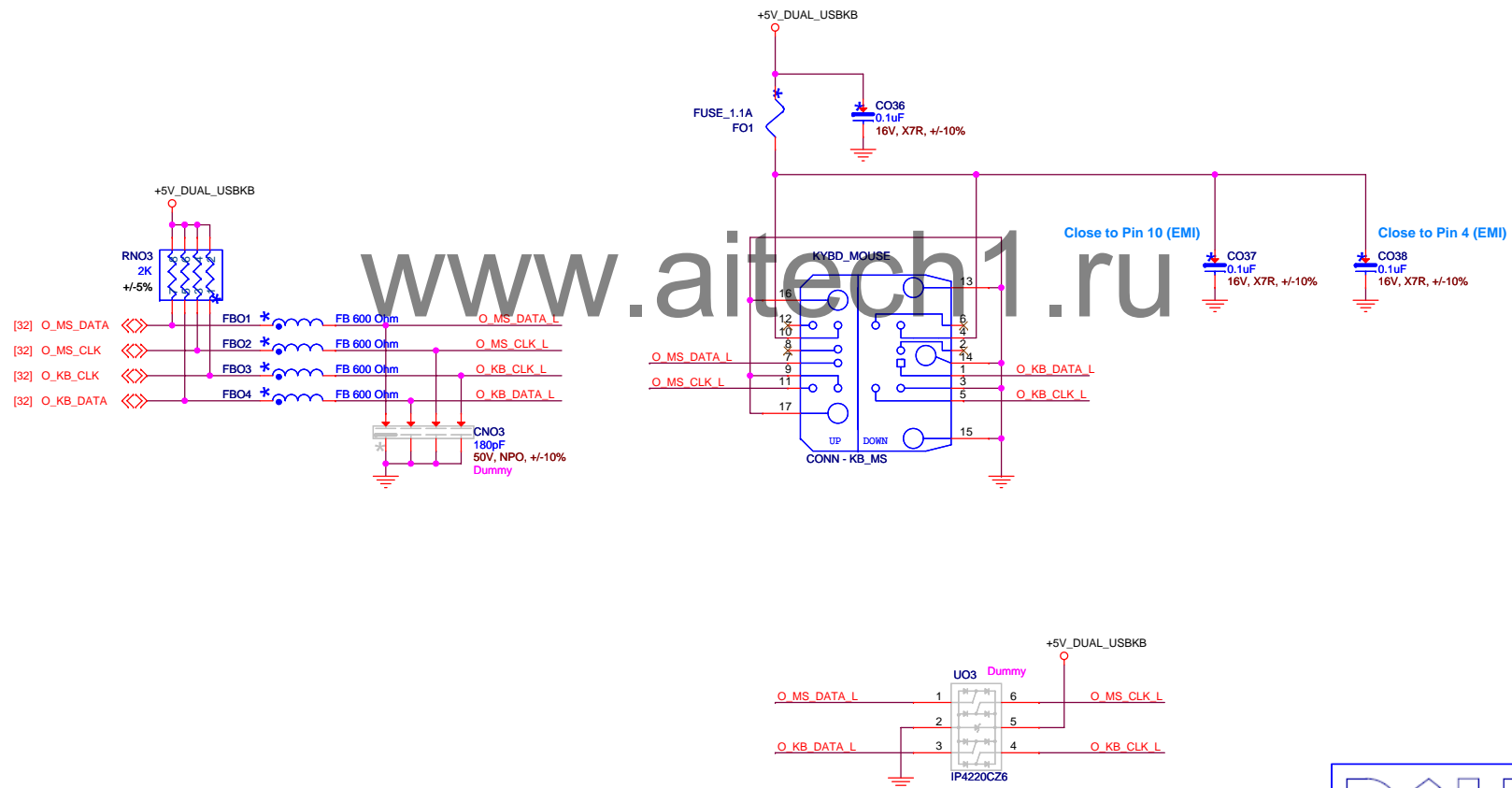
Title
FAN


DWG NO
Comoros

Rev
A01

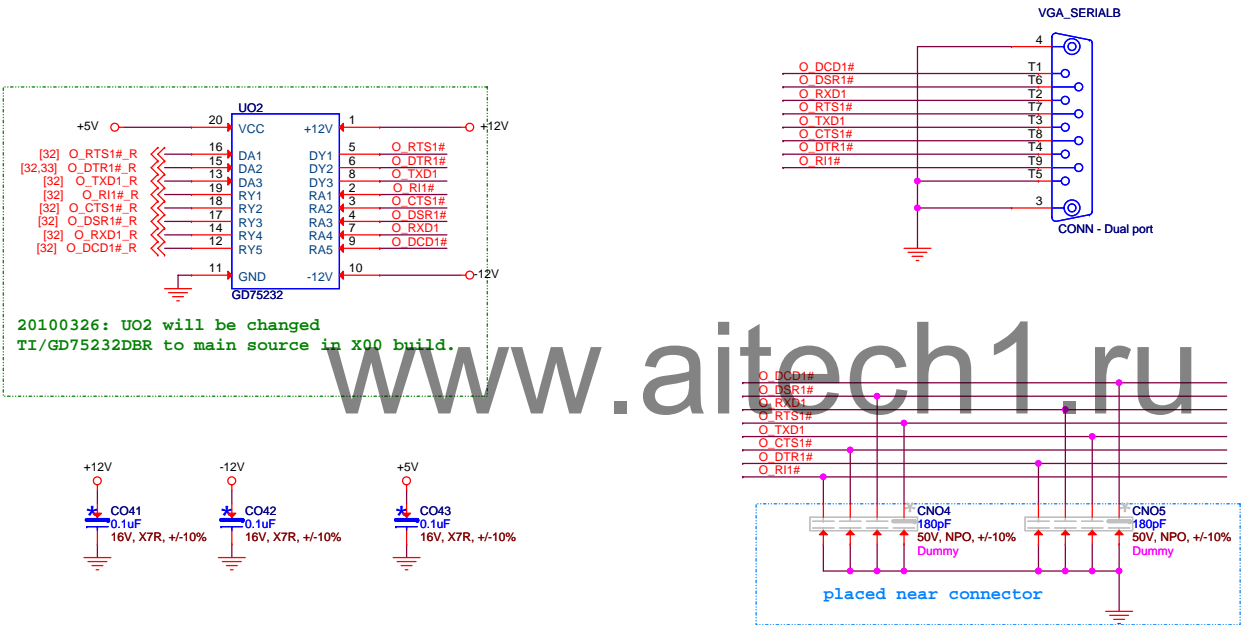
Date: Friday, November 30, 2012 Sheet 48 of 71

KB/MS



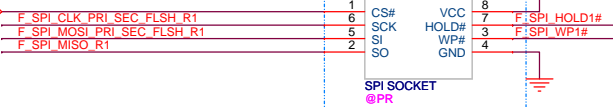
 INC.	
Title	
PS2 Conn	
DWG NO	Rev
Comoros	A01
Date: Friday, November 30, 2012	Sheet 49 of 71

Serial Port 1

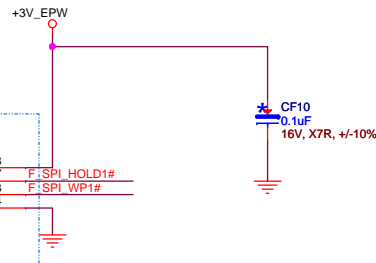


SPI

[24] F_SPI_CS1#_ISOLATE
20091225: Change net name for Dual SPI

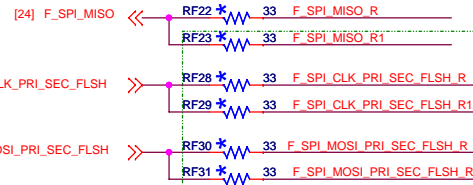
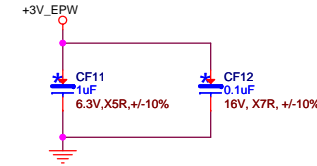
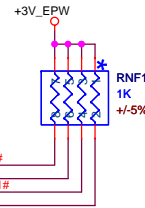


For debugging



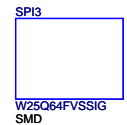
CLOSE TO SPI

If socket not use ,need change to SMD Tpye

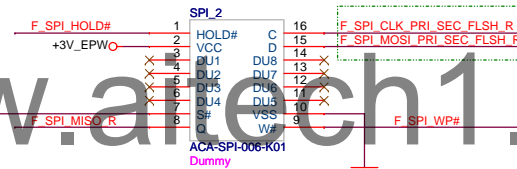


20091225: RF23 change to 33ohm for Dual SPI
20091225: Add RF28, RF29, RF30, RF31 for Dual SPI

[24] F_SPI_CS0#_ISOLATE

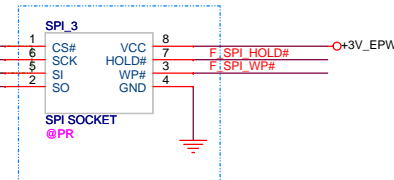


20091225: Change net name for Dual SPI



20091225: Change net name for Dual SPI

For debugging



Title

SPI

DWG NO

Comoros

Rev

A01

Date: Friday, November 30, 2012

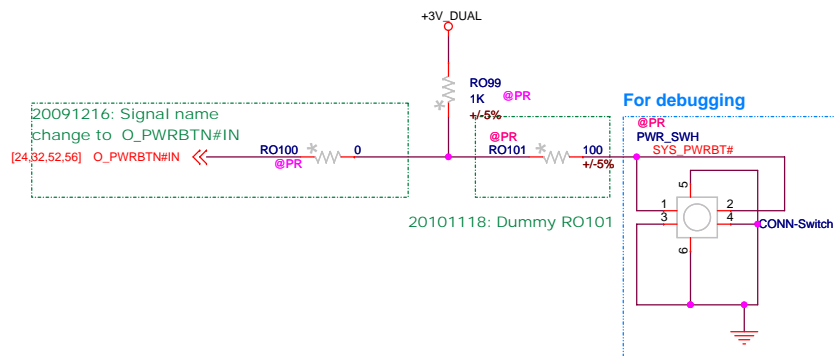
Sheet

51

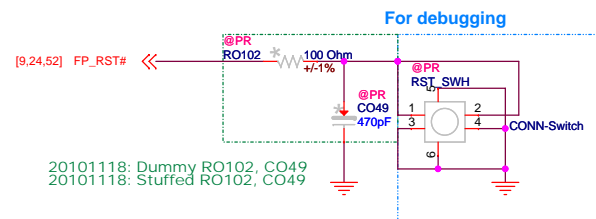
of

71

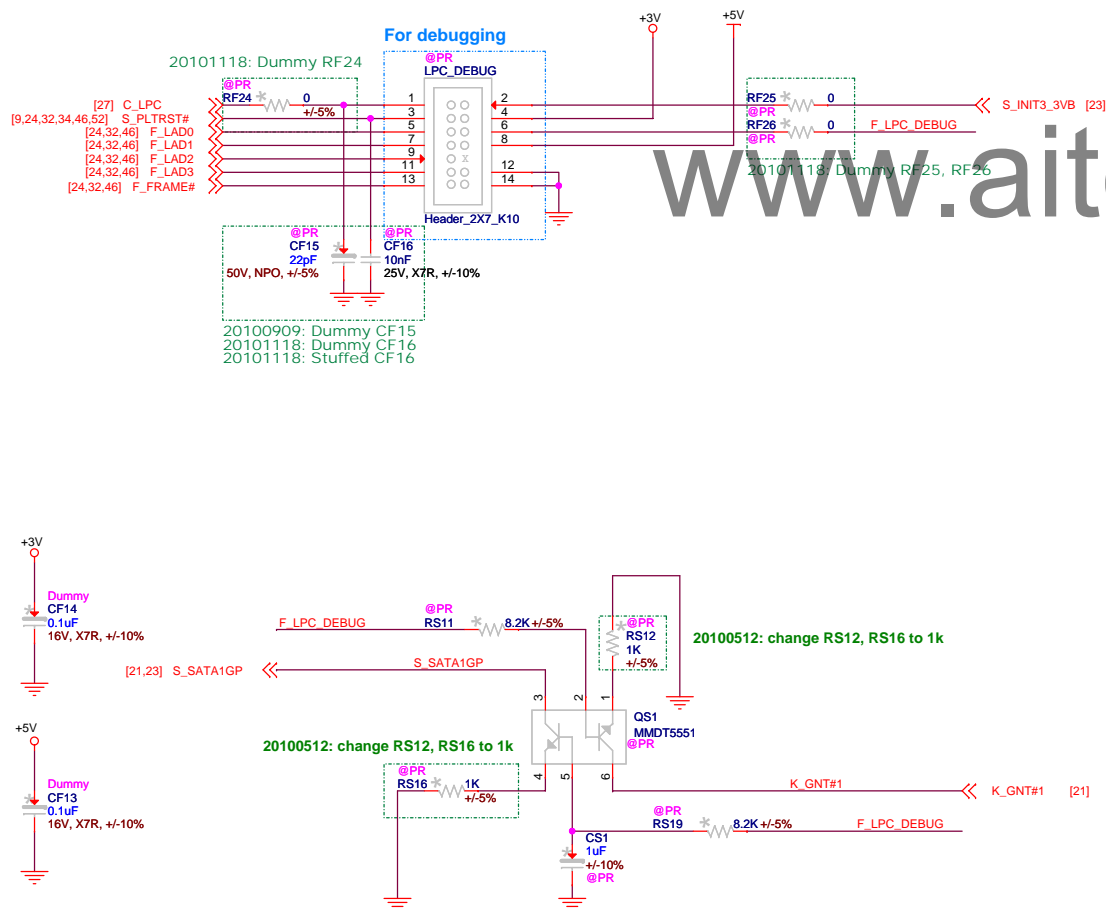
Power Bottom



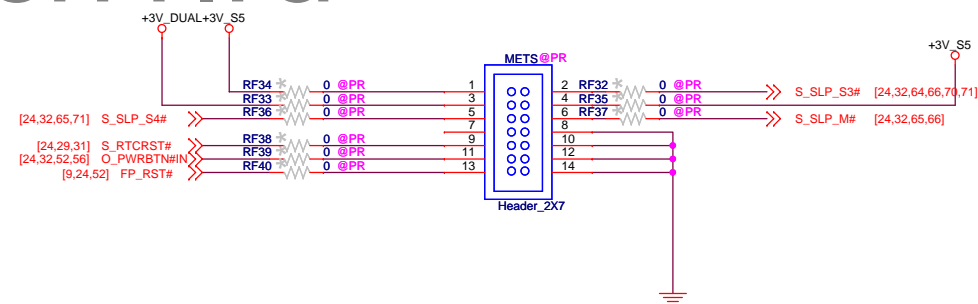
Reset Bottom



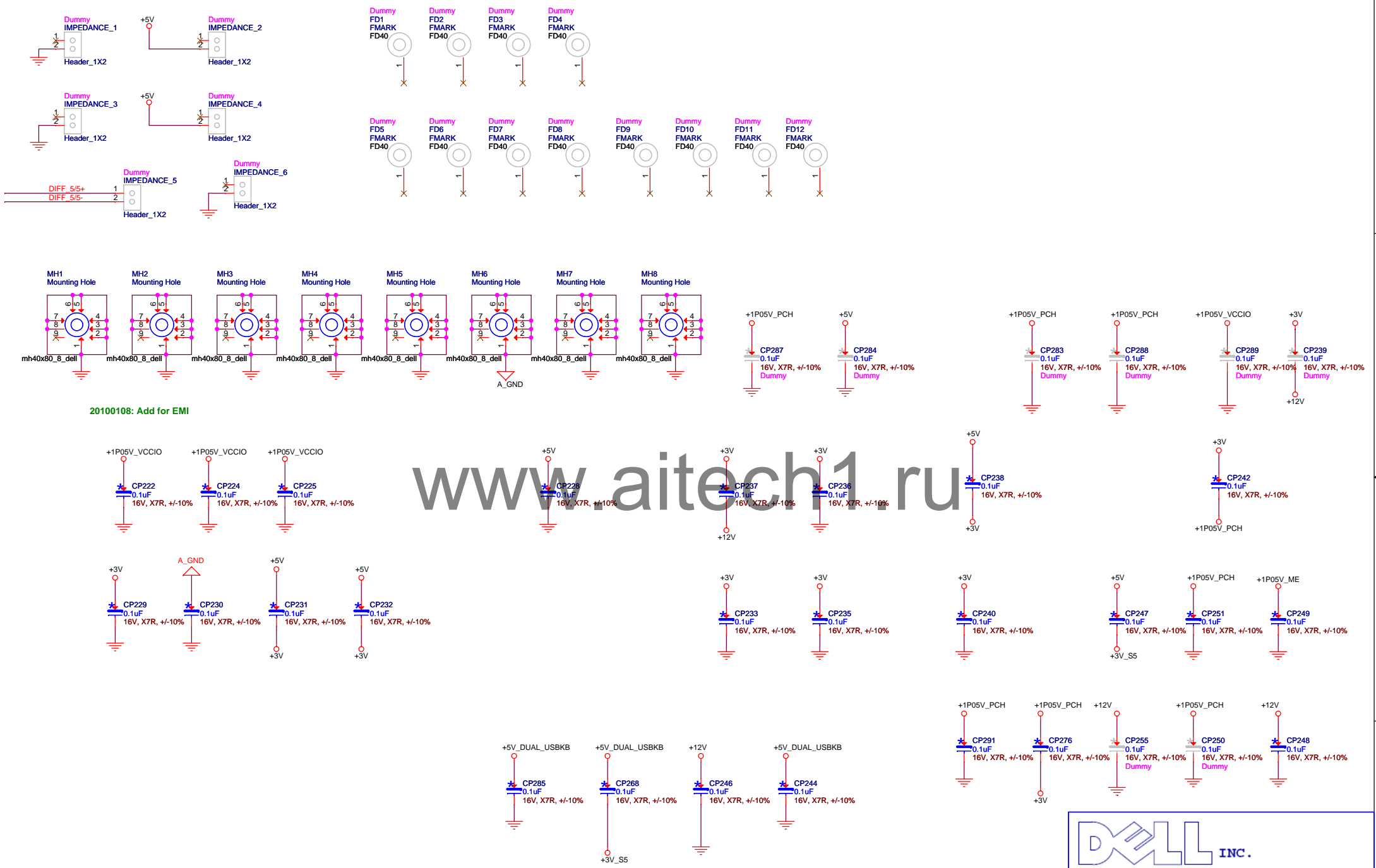
LPC DEBUG




APS Connector



		Title	
		Pilot Run Conn	
DWG NO	Comoros		Rev A01
Date: Friday, November 30, 2012	Sheet 53	of 71	

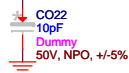
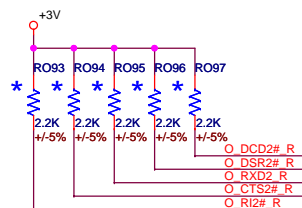


**INC.**

Title		
EMI		
DWG NO	Comoros	Rev
		A01
Date:	Friday, November 30, 2012	Sheet 54 of 71

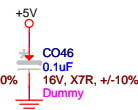
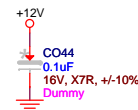
Move PWR_SW conn to
page56 20091126


Serial Port 2 Header



Dummy Serial Port2 header from X01

O_RI2#_R [32]



	
Title	
COM2 HDR	
DWG NO	Rev
Comoros	A01
Date: Friday, November 30, 2012	Sheet 55 of 71

Front USB/LED Header

Pitch 2.0mm

+3V

RNO2 8.2KOhm +/-5%

O_FIO_SATA_LED#

T_SATALED#

OQ14_C

S_FP_CHAS_DET#

[22] U_USB10N >>> RU38 0 Dummy U_USB10N_R

[22] U_USB10P >>> RU39 0 Dummy U_USB10P_R

[22] U_USB11N >>> RU41 0 Dummy U_USB11N_R

[22] U_USB11P >>> RU42 0 Dummy U_USB11P_R

20110212 Change to 2x13 for Front USB x2 port.

20110212 Change to 2x13 for Front USB x2 port.

MT/DT CHASSIS

FP_CHAS_DET#	MT/DT
0	MT
1	DT

FRONT PANEL

Header 2X10_K19

Header 2X3_K5

POWER SWITCH Header

Intel

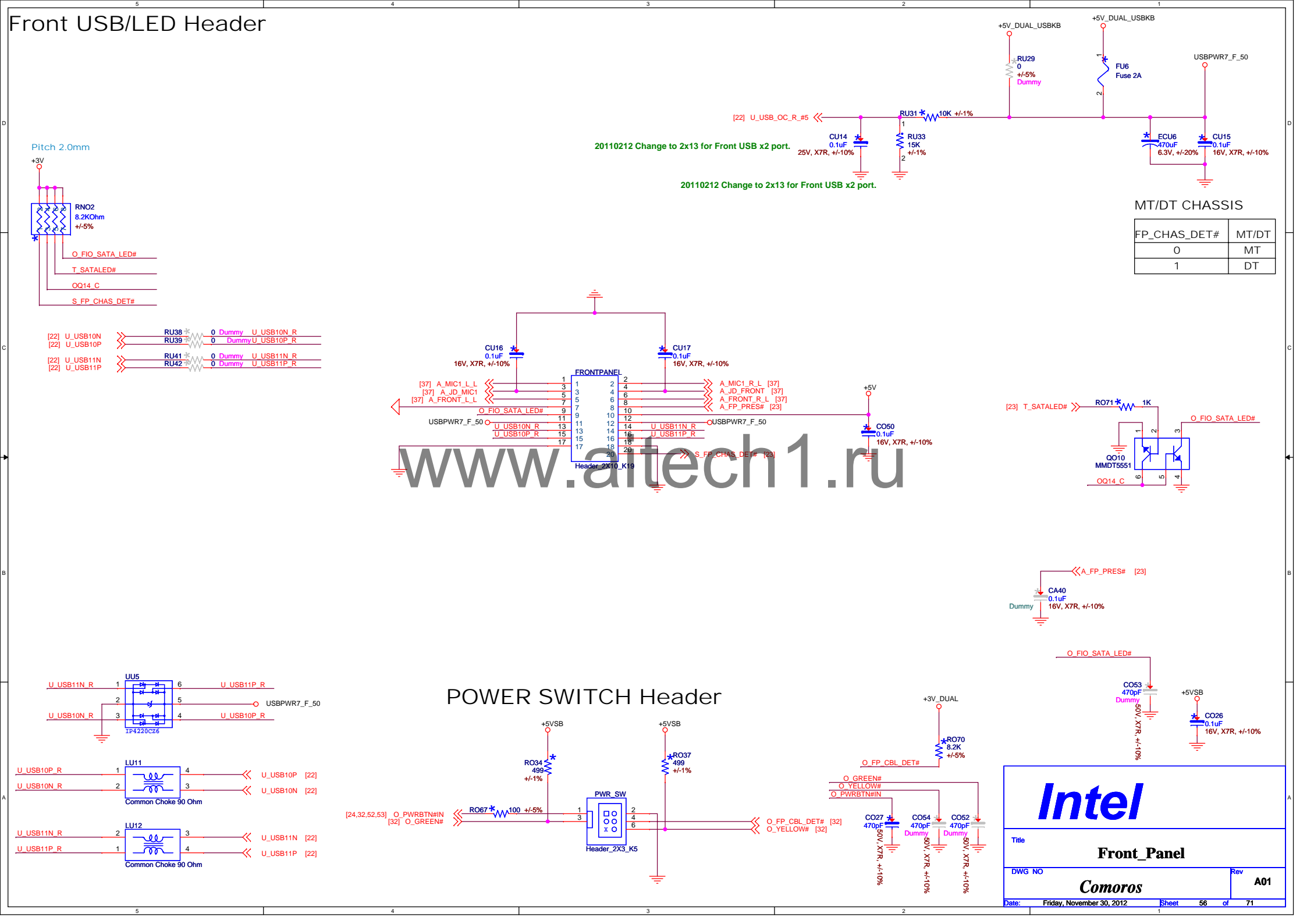
Front_Panel

Comoros

Rev A01

Date: Friday, November 30, 2012

Sheet 56 of 71



Front USB/LED Header

Pitch 2.0mm

+3V

RNO2 8.2KOhm +/-5%

O_FIO_SATA_LED#

T_SATALED#

OQ14_C

S_FP_CHAS_DET#

[22] U_USB10N >>> RU38 0 Dummy U_USB10N_R

[22] U_USB10P >>> RU39 0 Dummy U_USB10P_R

[22] U_USB11N >>> RU41 0 Dummy U_USB11N_R

[22] U_USB11P >>> RU42 0 Dummy U_USB11P_R

20110212 Change to 2x13 for Front USB x2 port.

20110212 Change to 2x13 for Front USB x2 port.

MT/DT CHASSIS

FP_CHAS_DET#	MT/DT
0	MT
1	DT

FRONT PANEL

Header 2X10_K19

Header 2X3_K5

POWER SWITCH Header

Intel

Front_Panel

Comoros

Rev A01

Date: Friday, November 30, 2012

Sheet 56 of 71

Front USB/LED Header

Pitch 2.0mm

+3V

RNO2 8.2KOhm +/-5%

O_FIO_SATA_LED#

T_SATALED#

OQ14_C

S_FP_CHAS_DET#

[22] U_USB10N >>> RU38 0 Dummy U_USB10N_R

[22] U_USB10P >>> RU39 0 Dummy U_USB10P_R

[22] U_USB11N >>> RU41 0 Dummy U_USB11N_R

[22] U_USB11P >>> RU42 0 Dummy U_USB11P_R

20110212 Change to 2x13 for Front USB x2 port.

20110212 Change to 2x13 for Front USB x2 port.

MT/DT CHASSIS

FP_CHAS_DET#	MT/DT
0	MT
1	DT

FRONT PANEL

Header 2X10_K19

Header 2X3_K5

POWER SWITCH Header

Intel

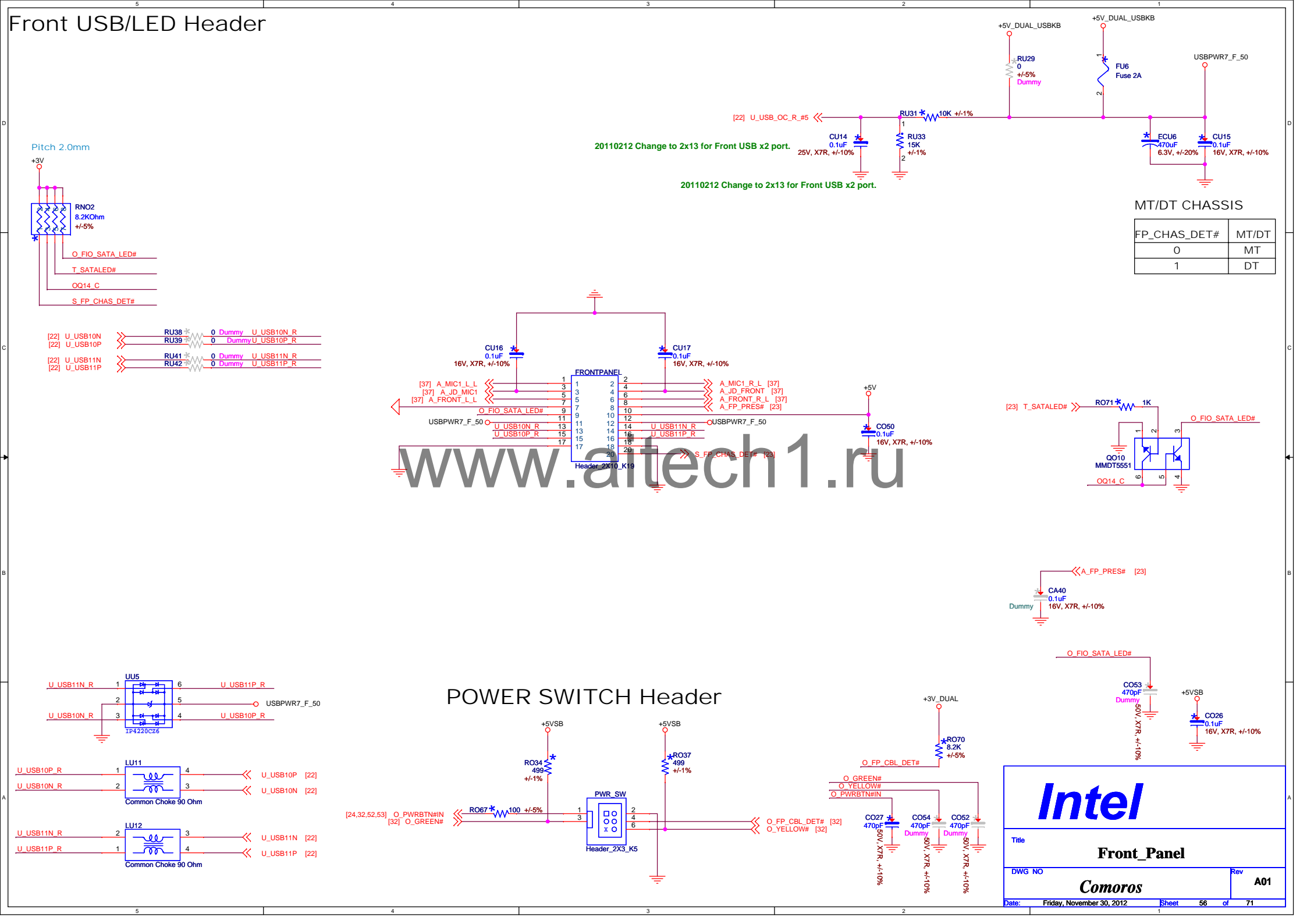
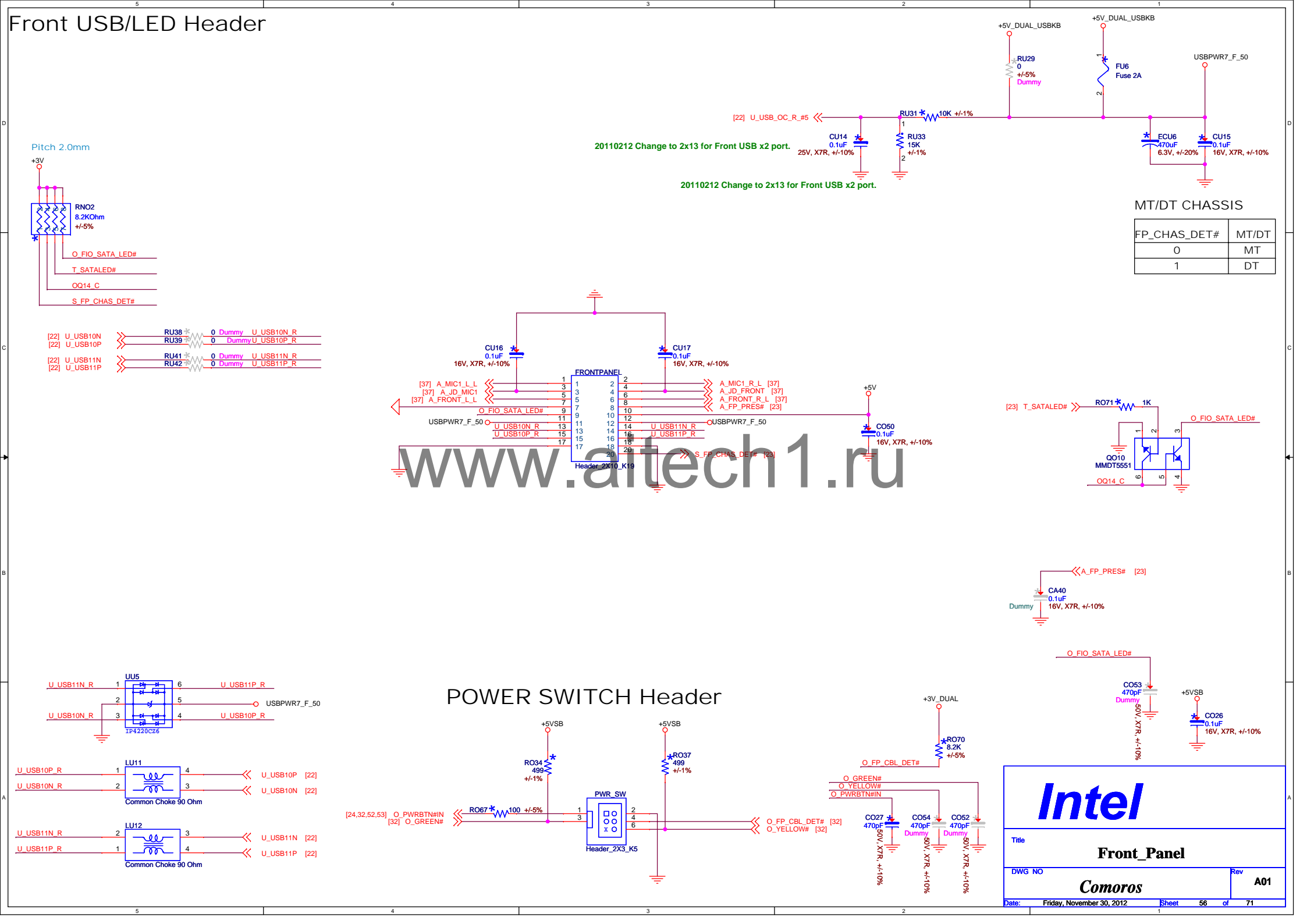
Front_Panel

Comoros

Rev A01

Friday, November 30, 2012

Sheet 56 of 71



Front USB/LED Header

Pitch 2.0mm
+3V

RNO2 8.2KOhm +/-5%

O_FIO_SATA_LED#
T_SATALED#
OQ14_C
S_FP_CHAS_DET#

[22] U_USB10N >> RU38 0 Dummy U_USB10N_R
[22] U_USB10P >> RU39 0 Dummy U_USB10P_R

[22] U_USB11N >> RU41 0 Dummy U_USB11N_R
[22] U_USB11P >> RU42 0 Dummy U_USB11P_R

CU16 0.1uF 16V, X7R, +/-10%
CU17 0.1uF 16V, X7R, +/-10%

FRONT PANEL

A_MIC1_L_L [37]
A_JD_MIC1 [37]
A_FRONT_L_L [37]

O_FIO_SATA_LED#
USBPWR7_F_50
U_USB10N_R [13]
U_USB10P_R [15]
U_USB11N_R [14]
U_USB11P_R [16]

S_FP_CHAS_DET# [23]

Header_2X10_K19

+5V

CO50 0.1uF 16V, X7R, +/-10%

[23] T_SATALED# >> RO71 1K

O_FIO_SATA_LED#

QO10 MMDT5551
OQ14_C

<< A_FP_PRES# [23]

Dummy CA40 0.1uF 16V, X7R, +/-10%

O_FIO_SATA_LED#

CO53 470pF 50V, X7R, +/-10%
CO26 0.1uF 16V, X7R, +/-10%

+5VSB

RO34 499 +/-1%
RO37 499 +/-1%

PWR_SW Header_2X3_K5

[24,32,52,53] O_PWRBTN#IN [32] O_GREEN#
[32] O_YELLOW#

RO67 100 +/-5%

O_FP_CBL_DET# [32]
O_YELLOW# [32]

O_FP_CBL_DET#

O_GREEN#
O_YELLOW#
O_PWRBTN#IN

CO27 470pF 50V, X7R, +/-10%
CO54 470pF 50V, X7R, +/-10%
CO52 470pF 50V, X7R, +/-10%

+3V_DUAL

RO70 8.2K +/-5%

O_FP_CBL_DET#

MT/DT CHASSIS

FP_CHAS_DET#	MT/DT
0	MT
1	DT

POWER SWITCH Header

U_USB11N_R 1 UU5 6 U_USB11P_R
U_USB10P_R 2 5 USBPWR7_F_50
U_USB10N_R 3 4 U_USB10P_R

IP4220C26

U_USB10P_R 1 LU11 4 U_USB10P [22]
U_USB10N_R 2 3 U_USB10N [22]

Common Choke 90 Ohm

U_USB11N_R 2 LU12 3 U_USB11N [22]
U_USB11P_R 1 4 U_USB11P [22]

Common Choke 90 Ohm

Intel

Front_Panel

DWG NO Comoros Rev A01

Date: Friday, November 30, 2012 Sheet 56 of 71

Front USB/LED Header

Pitch 2.0mm

+3V

RNO2 8.2KOhm +/-5%

O_FIO_SATA_LED#

T_SATALED#

OQ14_C

S_FP_CHAS_DET#

[22] U_USB10N >>> RU38 0 Dummy U_USB10N_R

[22] U_USB10P >>> RU39 0 Dummy U_USB10P_R

[22] U_USB11N >>> RU41 0 Dummy U_USB11N_R

[22] U_USB11P >>> RU42 0 Dummy U_USB11P_R

20110212 Change to 2x13 for Front USB x2 port.

20110212 Change to 2x13 for Front USB x2 port.

MT/DT CHASSIS

FP_CHAS_DET#	MT/DT
0	MT
1	DT

FRONT PANEL

Header 2X10_K19

Header 2X3_K5

POWER SWITCH Header

Intel

Front_Panel

Comoros

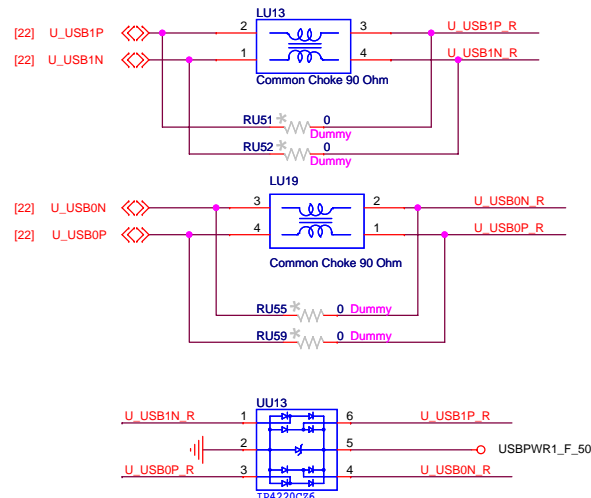
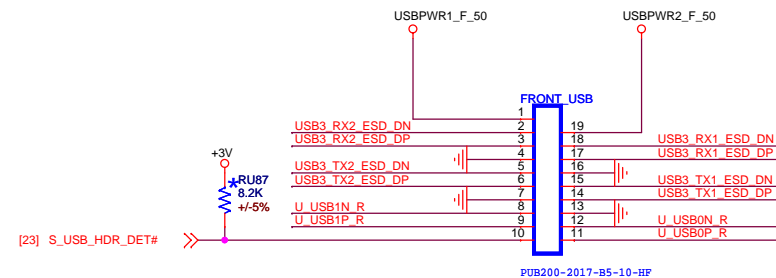
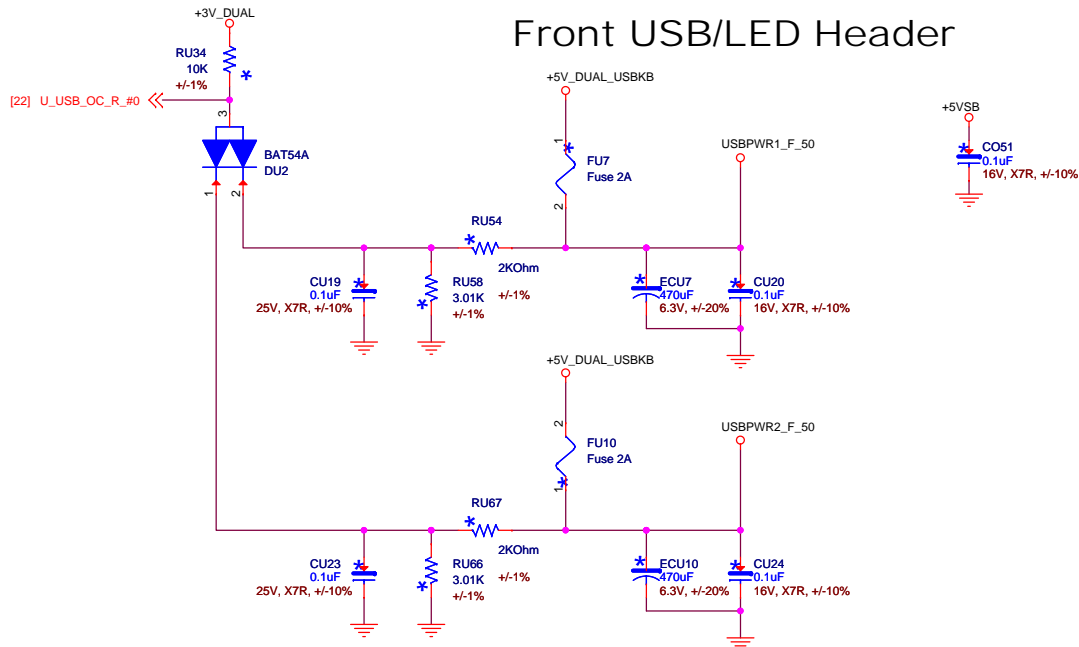
Rev A01

Date: Friday, November 30, 2012

Sheet 56 of 71

[illegible][illegible]

Front USB/LED Header



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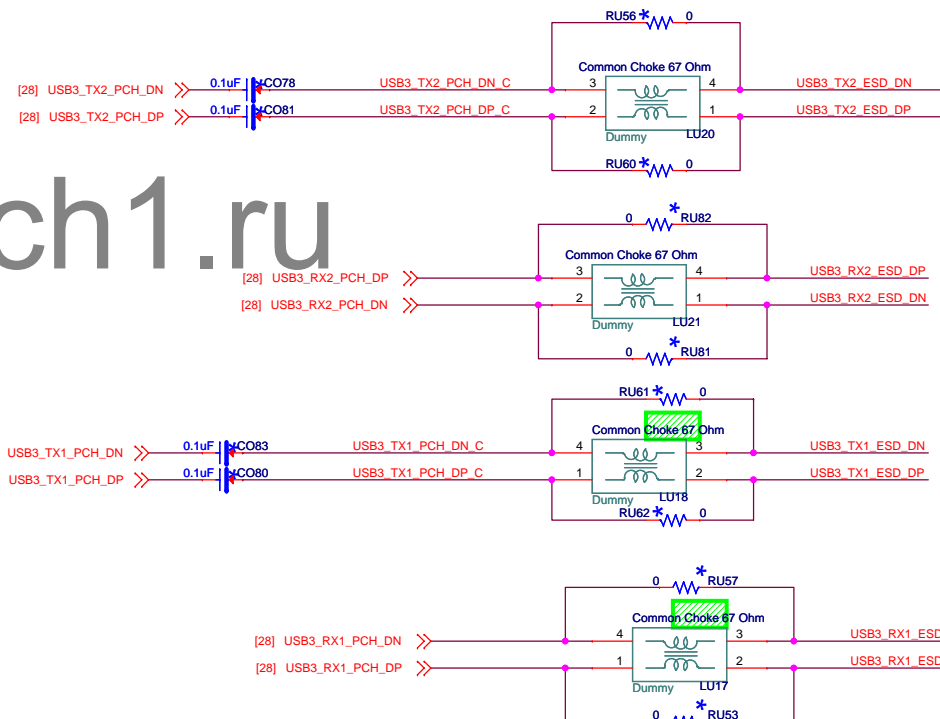
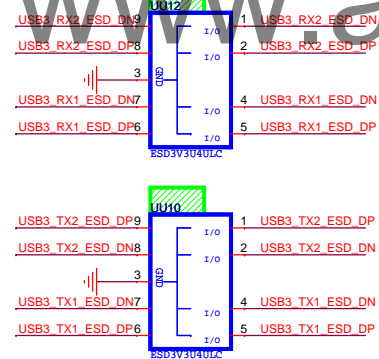
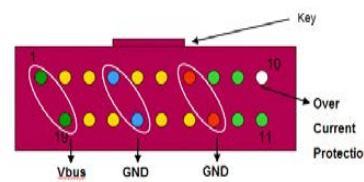


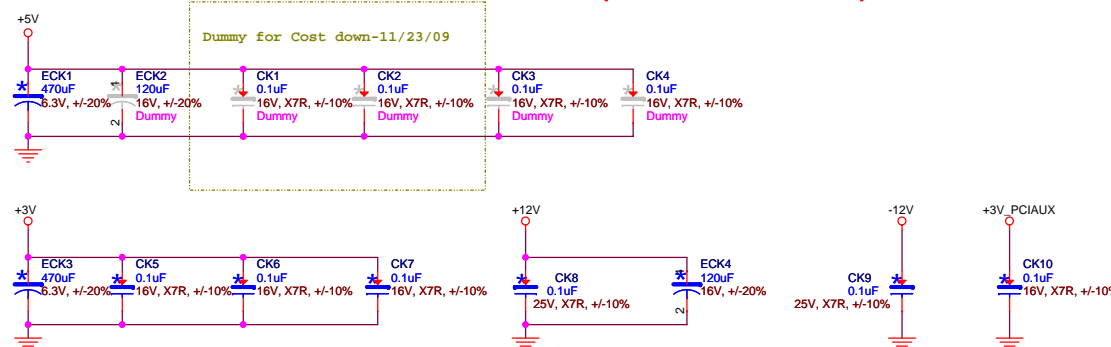
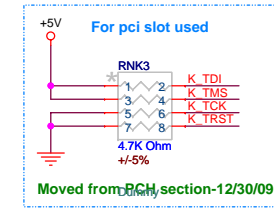
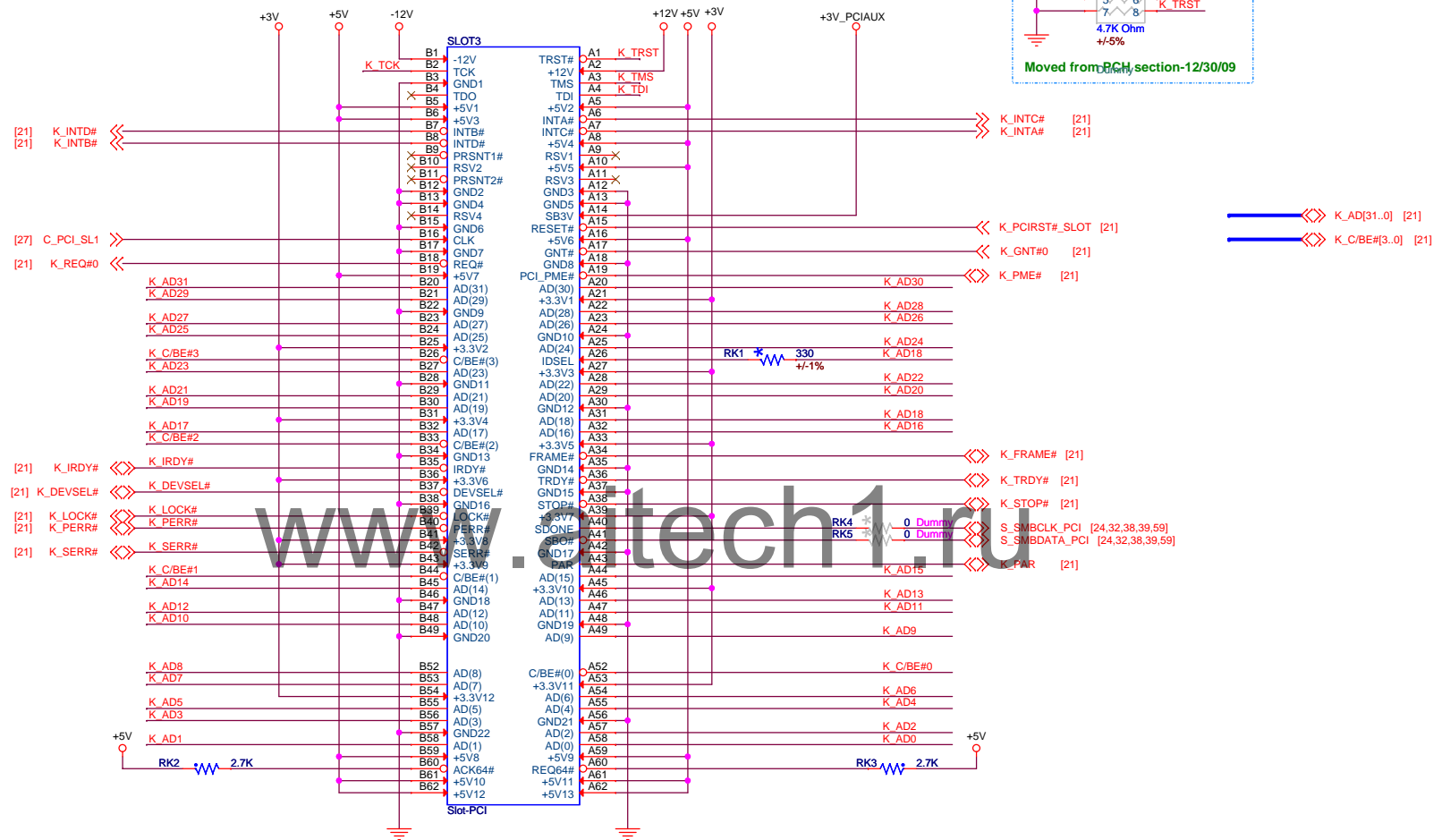
Figure 2-1: USB3 IC pin numbering



Intel

Title		TBD	
DWG NO		Rev	A01
Date:	Friday, November 30, 2012	Sheet	57 of 71

IRQ: CDAB
IDSEL: AD18
REQ/GNT: 0

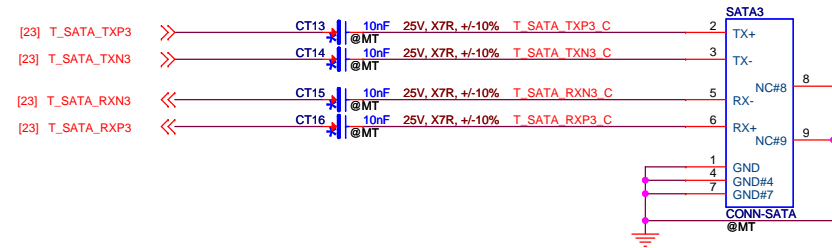



DELL INC.	
Title	
Slot3: PCI	
DWG NO	Rev
Comoros	A01
Date: Friday, November 30, 2012	Sheet 58 of 71



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SATA port 3 only for MT



 **INC.**

SATA_MT

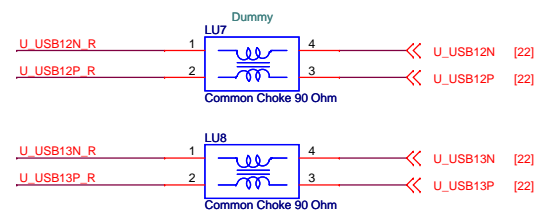
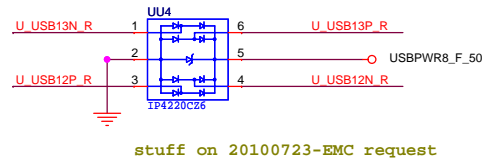
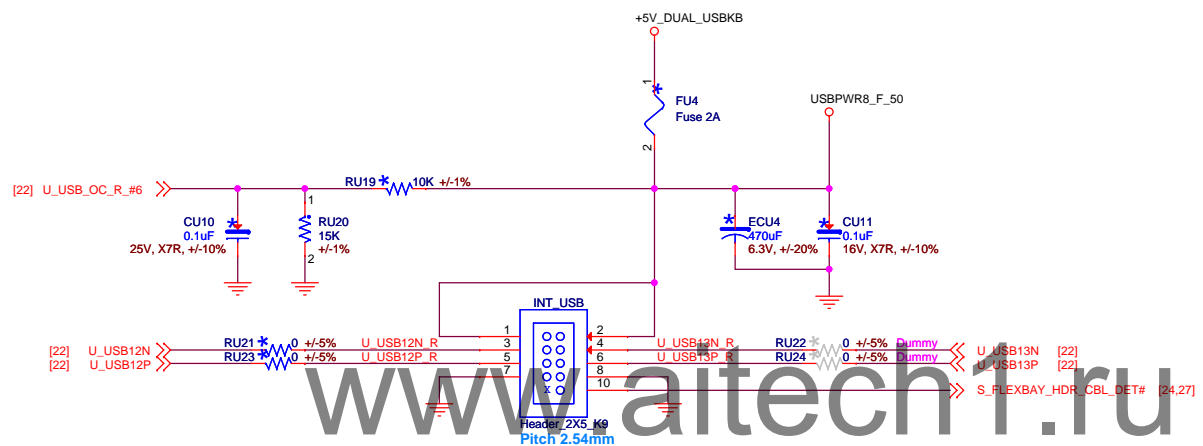
DWG NO

Comoros

Rev

A01

Date: Friday, November 30, 2012Sheet 60 of 71



CO-LAY with 4 Serial resistors RU21, RU22, RU23, & RU24

Title

Flexbay USB_MT

DWG NO

Comoros


Rev

A01

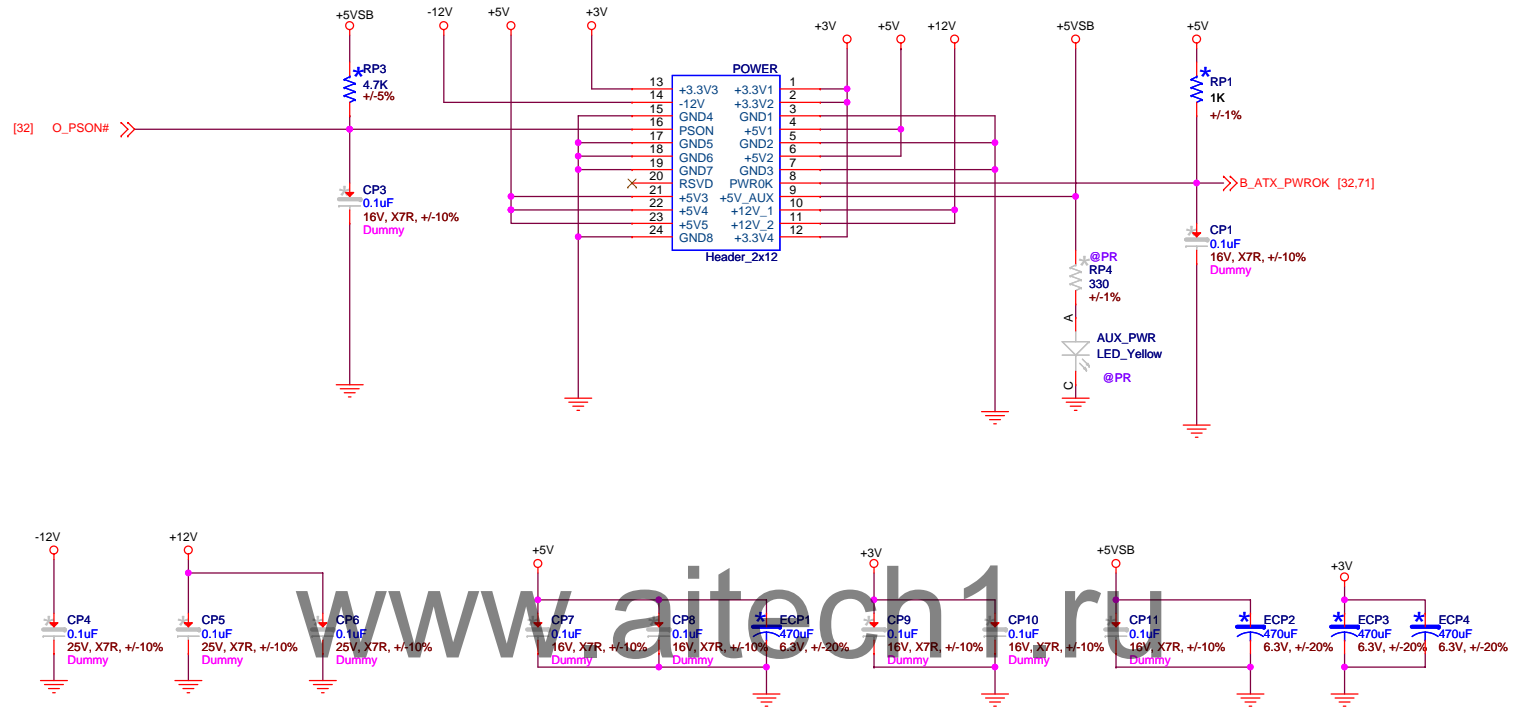
Date: Friday, November 30, 2012

Sheet 61 of 71

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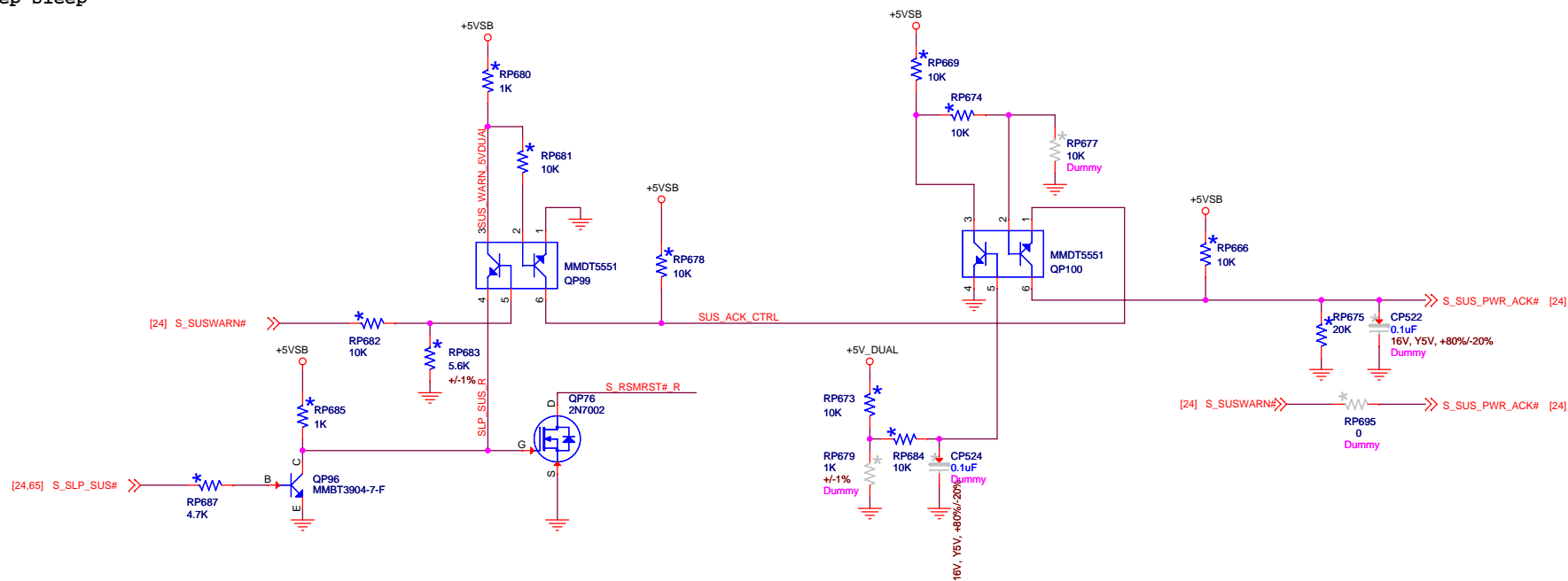
	
Title PRT Port	
DWG NO <i>Lanikai_MT/DT</i>	Rev A01
Date: Friday, November 30, 2012	Sheet 62 of 71

ATX POWER CONNECTOR

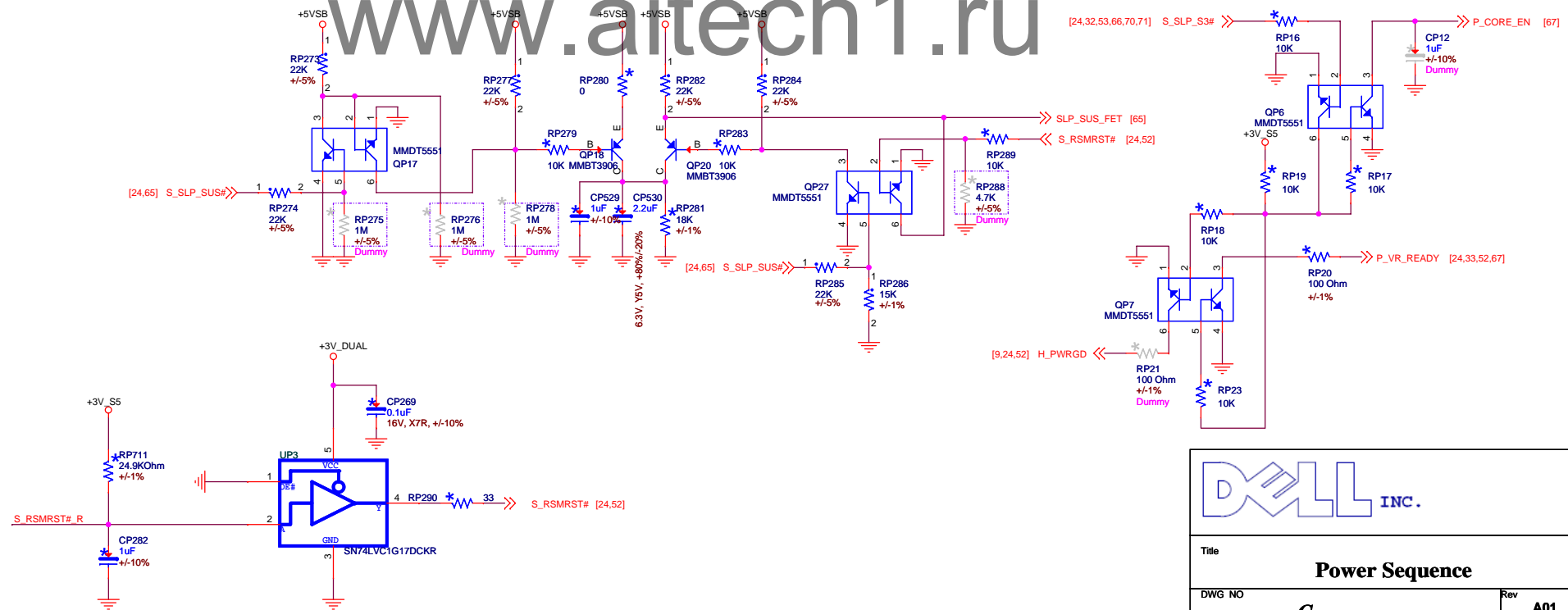


Title		
Power Conn		
DWG NO	Rev	A01
Comoros		
Date: Friday, November 30, 2012	Sheet 63	of 71

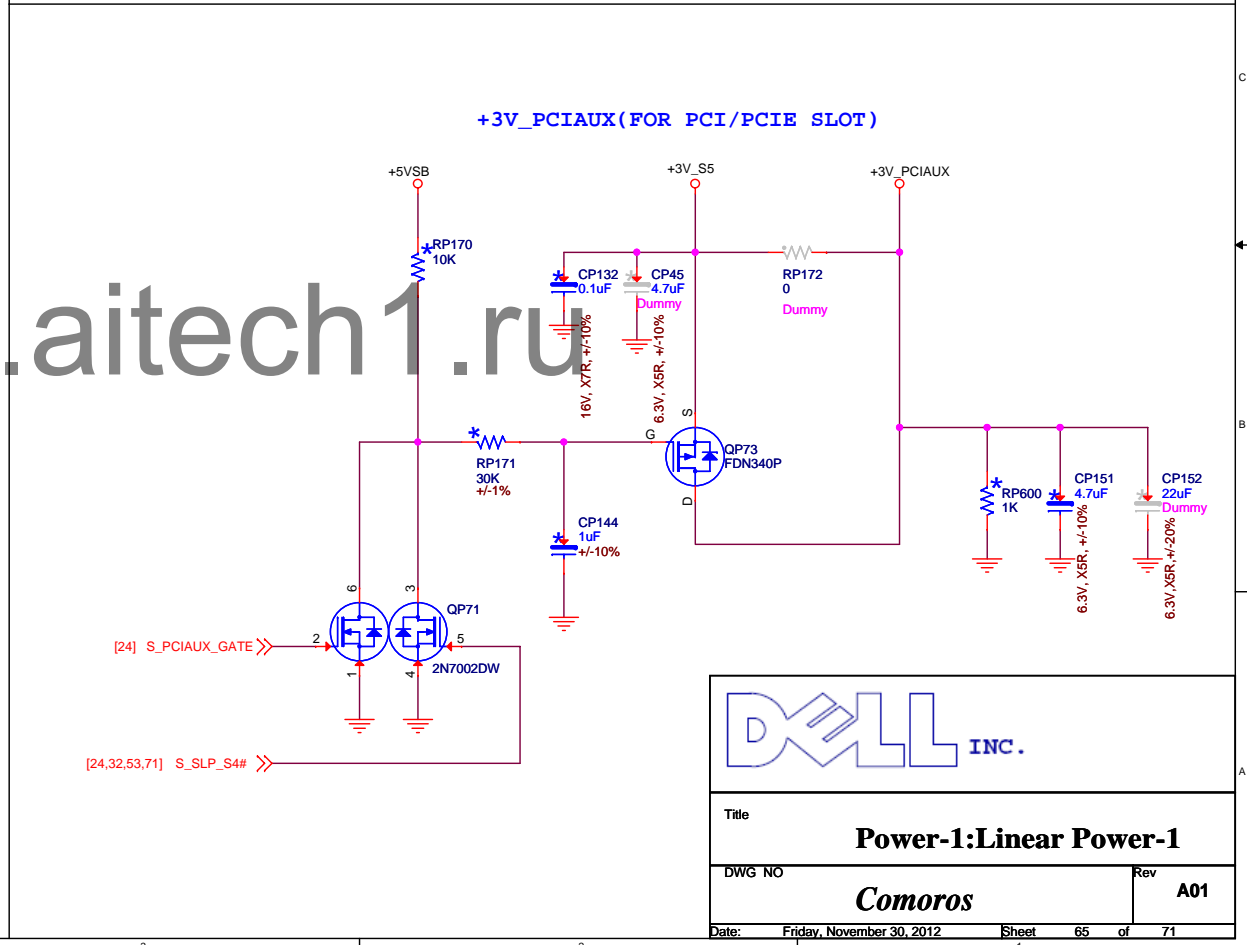
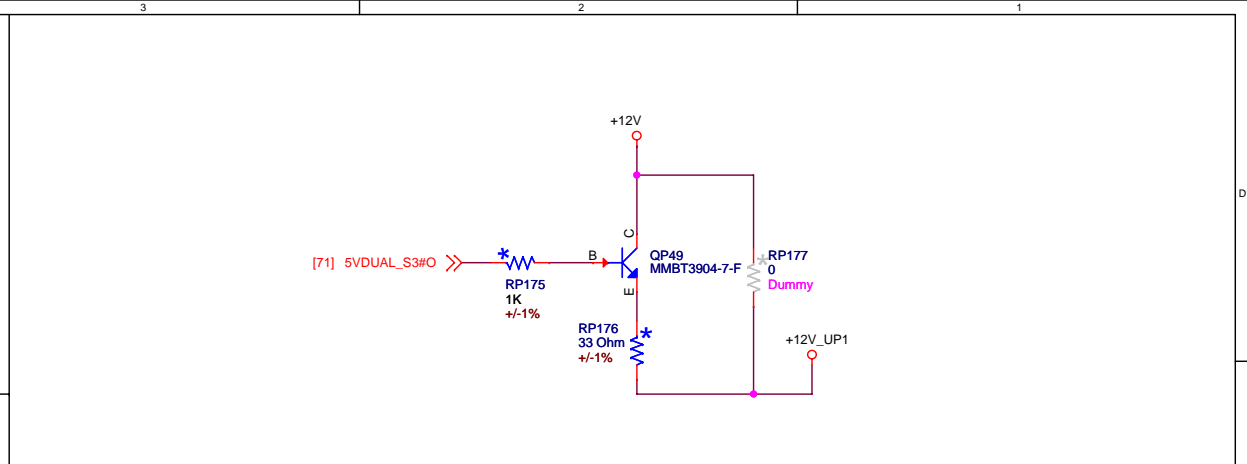
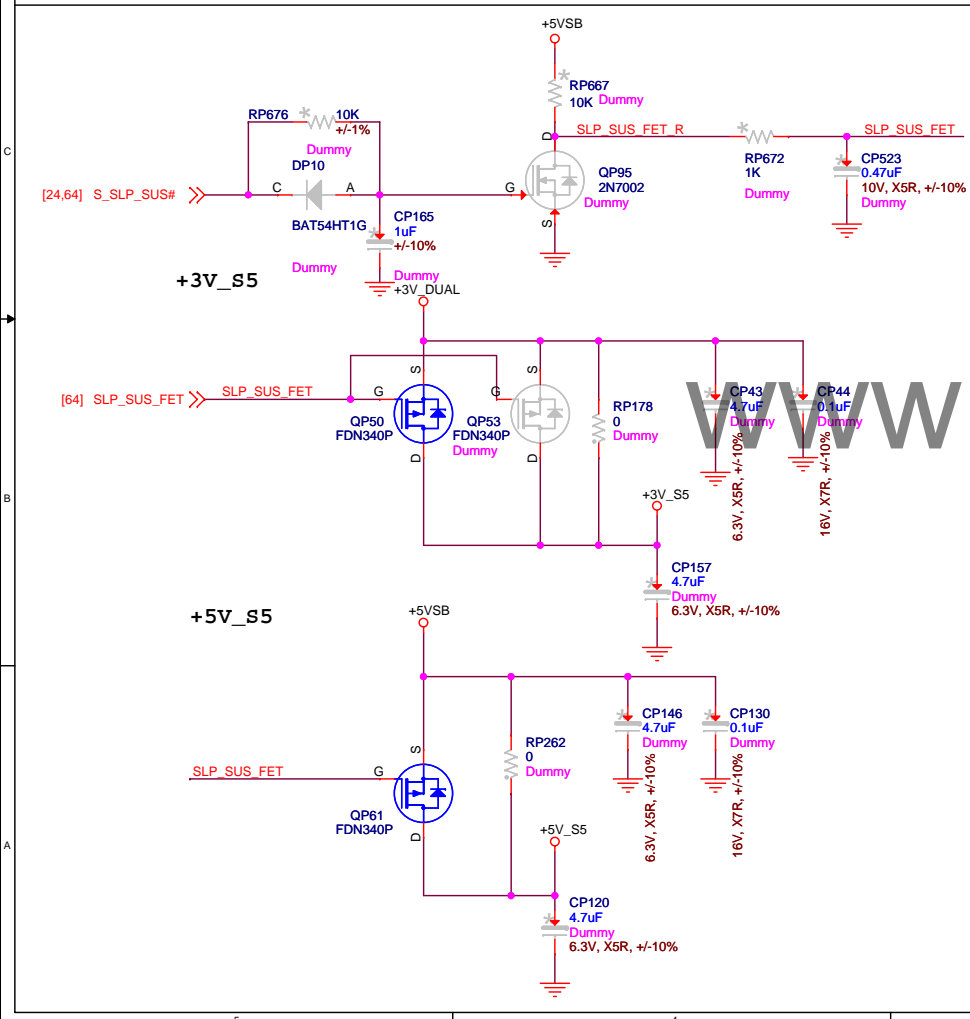
For Deep Sleep



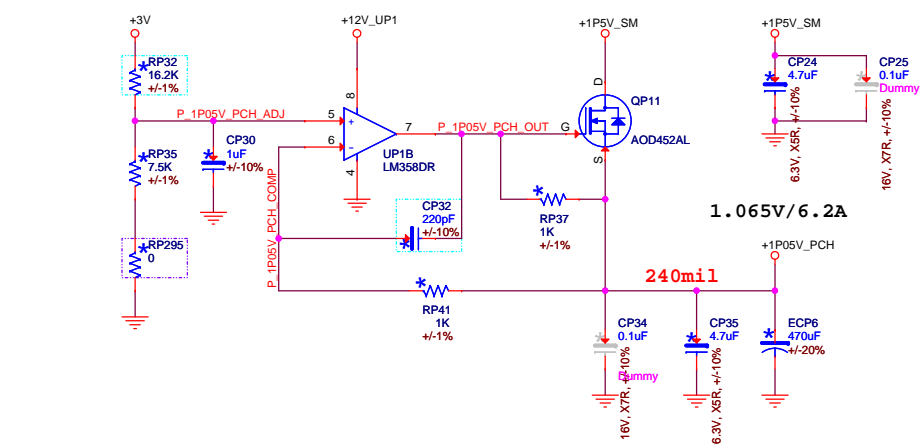
RESUME RESET Logic



Title	
Power Sequence	
DWG NO	Rev
<i>Comoros</i>	A01
Date: Friday, November 30, 2012	Sheet 64 of 71



+V_1.05_PCH



**+V_1.05_PCH
ENABLE CIRCUIT**

4,32,53,64,70,71] S_SLP_S3#

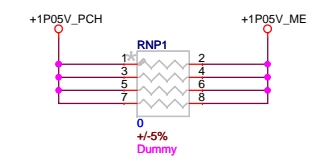
RP48 10K

RP47 10K

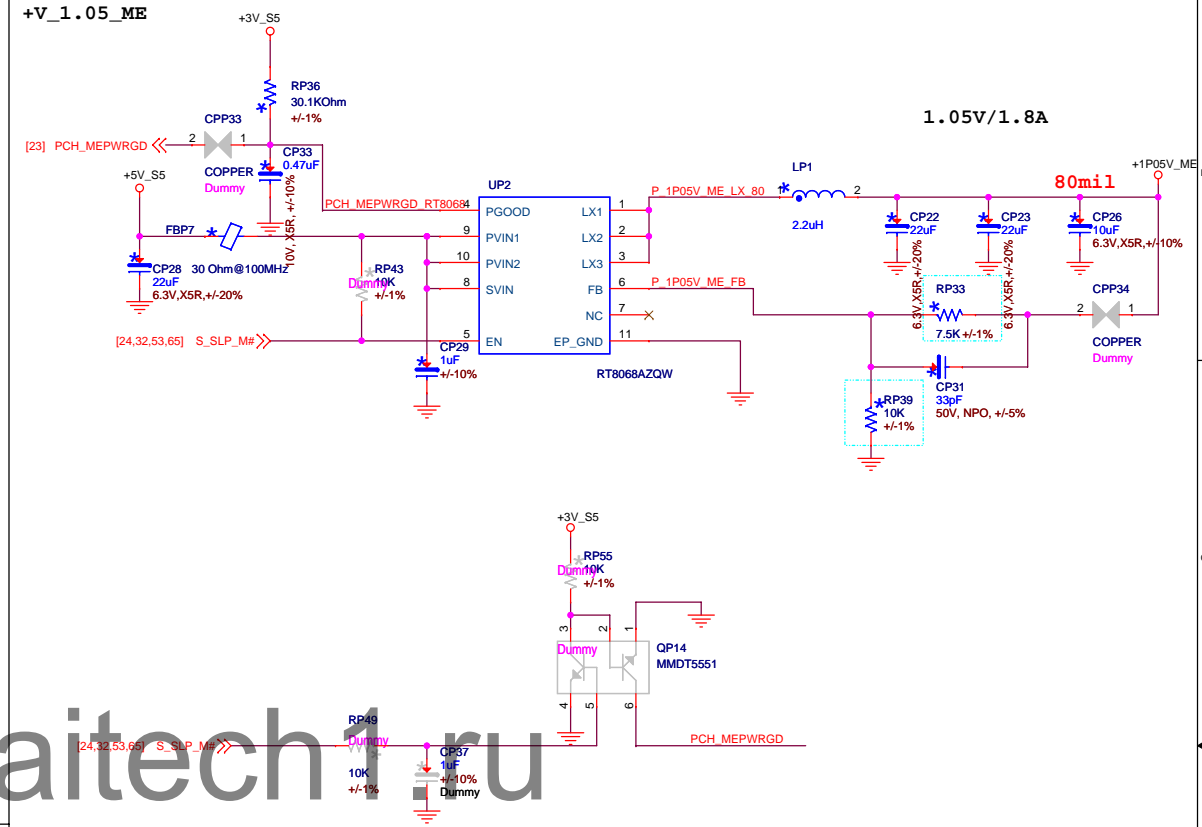
QP16 MMBT3904-7-F

QP15 2N7002

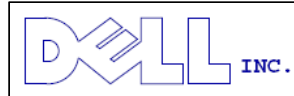
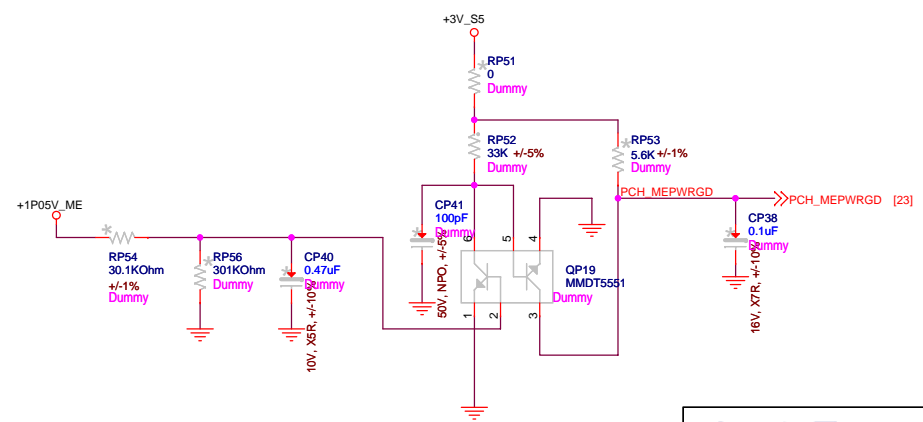
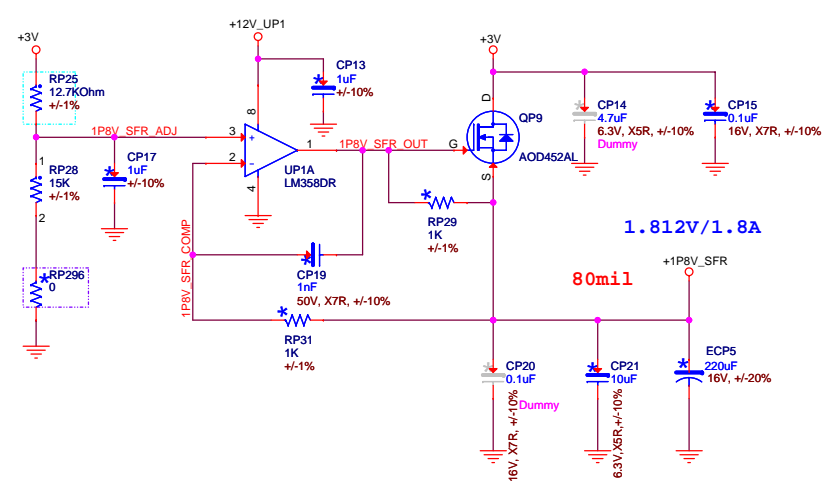
P 1P05V_PCH_ADJ



+V_1.05_ME



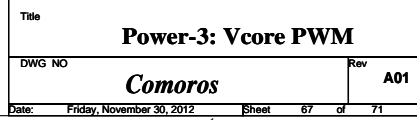
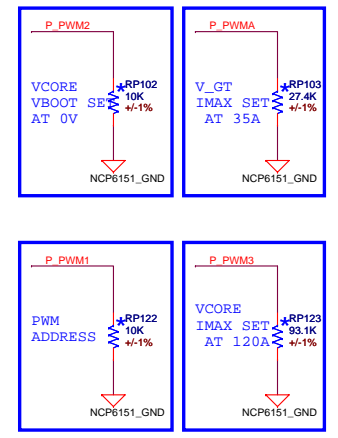
+V_1P8_SFR

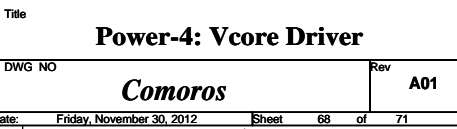


Title	Power-2:Linear Power-2
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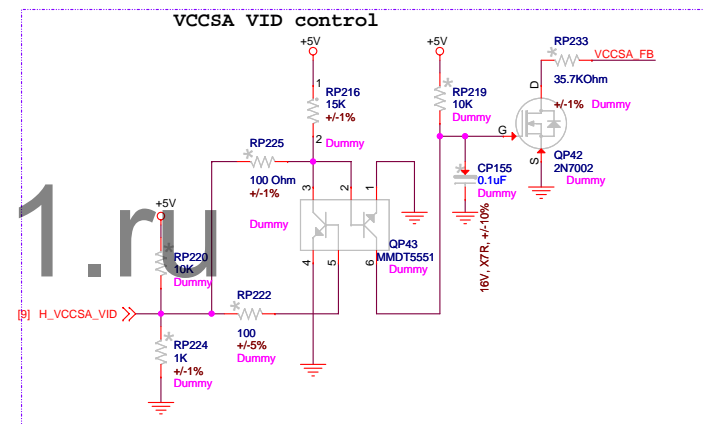
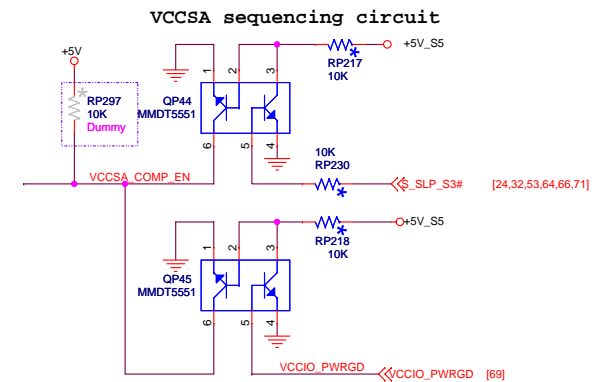
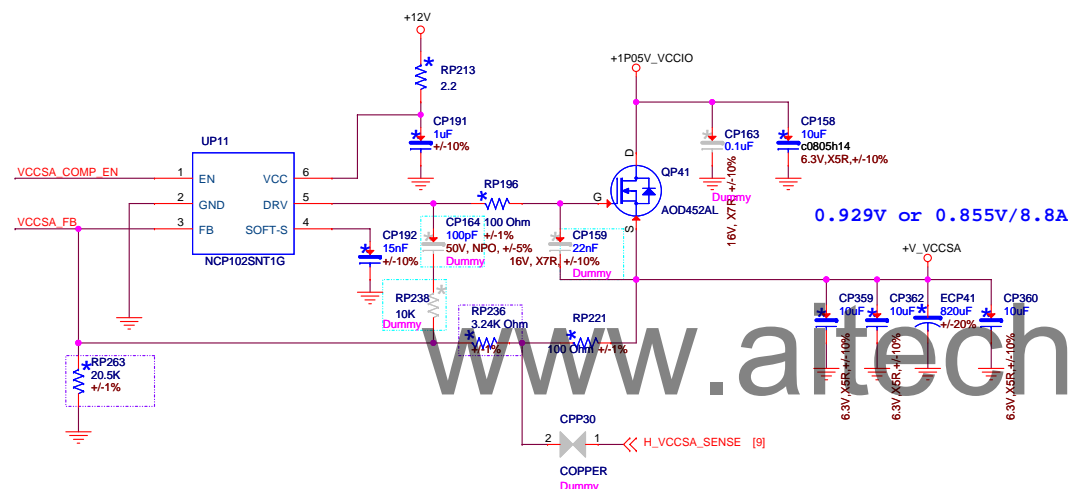
DWG NO	<i>Comoros</i>	Rev	A01
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VCC_AXG

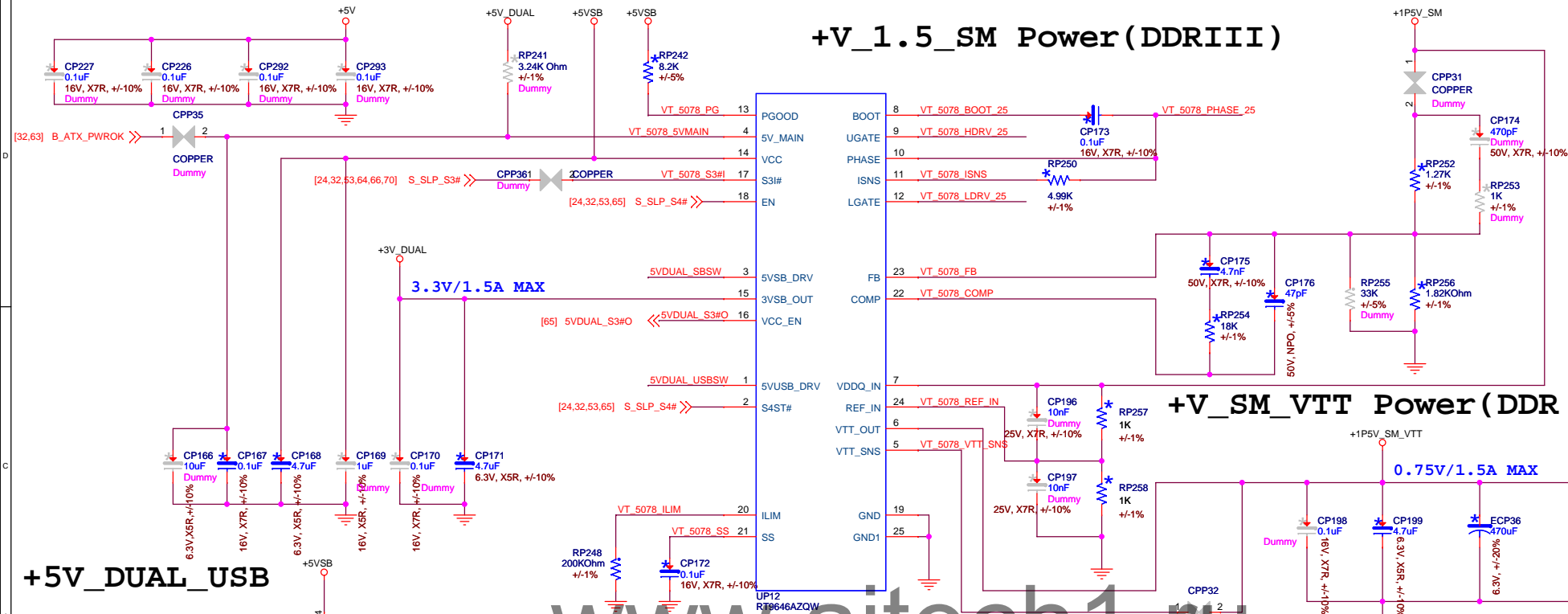




71

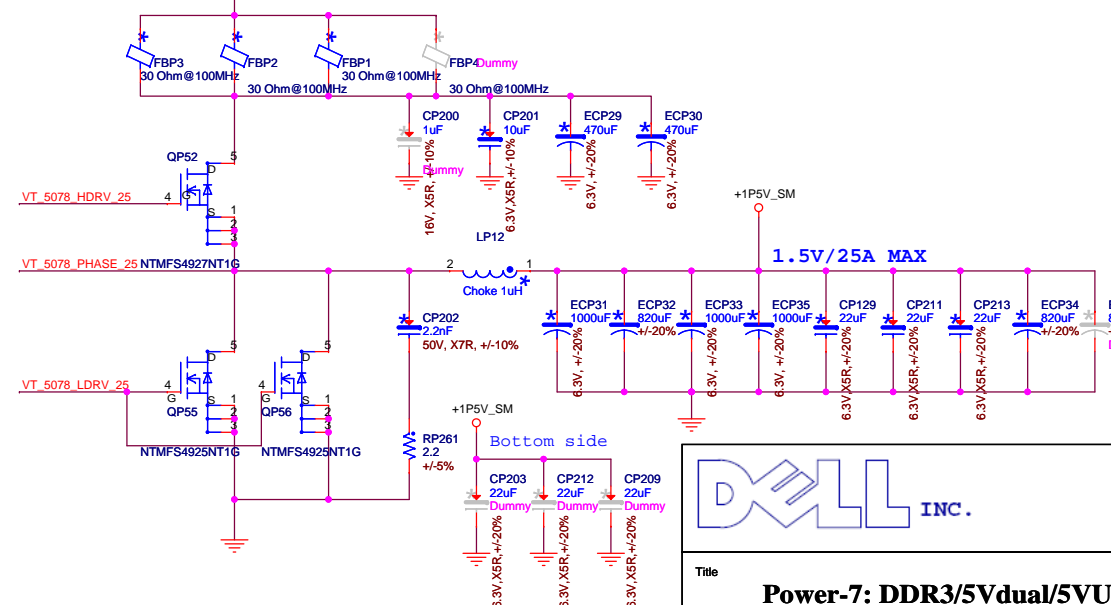


+V_1.5_SM Power (DDRIII)



+V_SM_VTT Power (DDR VTT)

+V_1.5_SM Power (DDRIII)



Title		
Power-7: DDR3/5Vdual/5VUSB		
DWG NO	Rev	A01
Comoros		
Date: Friday, November 30, 2012	Sheet	71 of 71

Max. output current = 1.5A